

Interface between SysML and Sequence Planner Language for Formal Verification

Peter Falkman (Chalmers University of Technology) - petter.falkman@chalmers.se
Joakim Berglund (Chalmers University of Technology) - berglunj@student.chalmers.se
Petter Falkman (Chalmers University of Technology) - petter.falkman@chalmers.se
Bengt Lennartson (Chalmers University of Technology) - bengt.lennartson@chalmers.se

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Abstract. This paper presents a method and software for interfacing Systems Modeling Language (SysML) and Sequence Planner Language (SPL). Exchange of information between different software tools is of major interest for modern manufacturing industries from early design to final implementation. SysML, with its structure as a common platform, can then be interfaced with other domain-specific modeling tools to achieve information exchange. This paper presents a method to interface SysML with a recently introduced language for operation sequences called Sequence Planner Language (SPL). By this method, necessary information from behavioral constructs of SysML model are extracted and structured in SPL. This language, being a formal, graphical language, can be used to formally verify the system for any blocking states. An academic and an industrial model developed in SysML are tested using the interface implementation and the results show that information from SysML can be visualized in SPL and formally verified to have no blocking states.