

IV&V

8/12/2024

INCOSE Chapter Meeting - CJD

Past

Origin Story: Truth, Validity, and Syllogism

Aristotle: 350 BCE

Truth: (Veritas, Verification) a relationship between a single proposition and the real world, or the nature of things, or "objective reality," or what is "outside of" (independent of) the proposition and the mind that expresses it.

Validity: (Value, Validation) a relationship between propositions: between the premises of an argument and the conclusion of the arguments

Syllogism: (Integration) Argument with three propositions, two premises, and one conclusion

Ref: Pages 194 and 215 of Socratic Logic - Peter Kreeft Edition 3.1

Examples from [Socratic Logic](#) with some potential fallacies:

1. The earth is a star
And no stars are fish
Therefore, the earth is not a fish

2. All men are mortal
And all pigs are mortal
Therefore, all pigs are men

3. All men are mortal
And Socrates is a man
Therefore, Socrates is mortal

“Developing a Theoretical Basis for Validation in Systems Engineering”

The Proceedings of
the 2024 Conference
on Systems
Engineering Research

- "there are acceptable practices/guidelines for translating needs to requirements, but **there is lack of theoretical foundations that serve as a basis to claim that a system is valid.**"
- "Specifically, this paper has focused on formally characterizing validation in systems engineering in terms of SE artifacts including stakeholders' needs, requirements, design, and verification. Formal definitions for validities associated with the artifacts and the overall system were provided **using propositional logic as the foundation**. The logical notions of logical **validity**, **soundness**, and **consistency** were used to define the different validities."

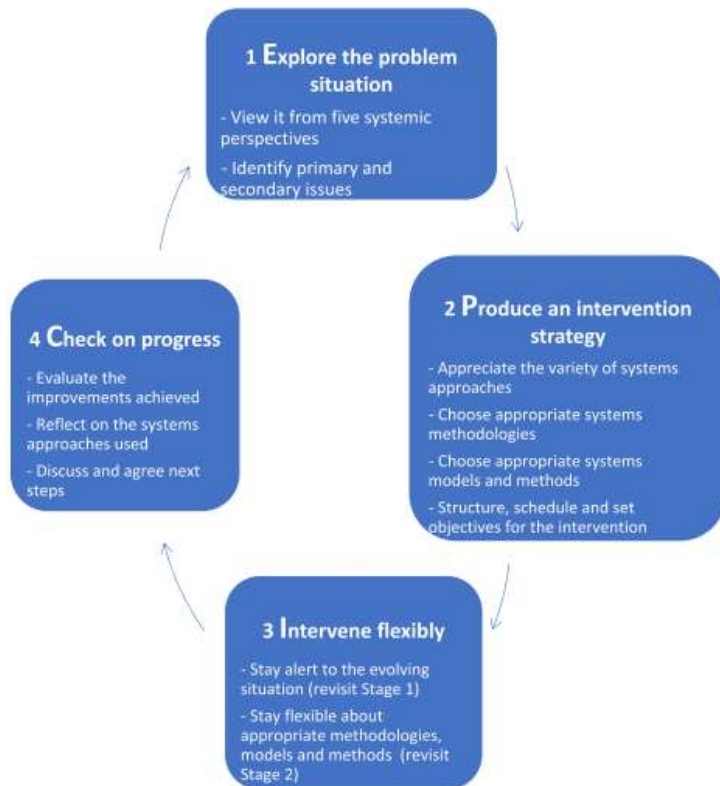
The Proceedings of the 2024 Conference on Systems Engineering Research, Conference on Systems Engineering Research Series, https://doi.org/10.1007/978-3-031-62554-1_10

H. Kannan, B. Davis, The University of Alabama in Huntsville, Huntsville, AL, USA, M. Suresh Kumar Virginia Tech, Blacksburg, VA, USA

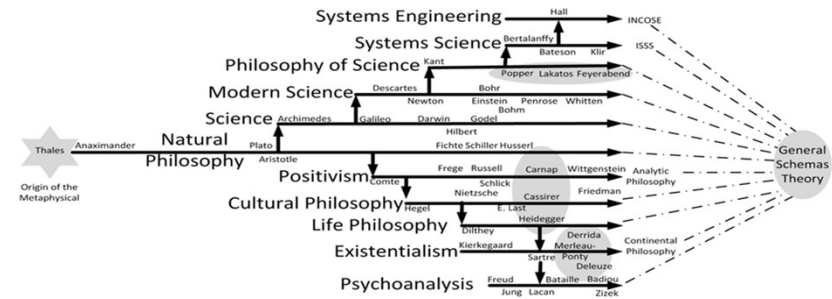
Other Philosophies underpinning what is “Valid”

Five Systemic Perspectives (Michael C. Jackson 2019):

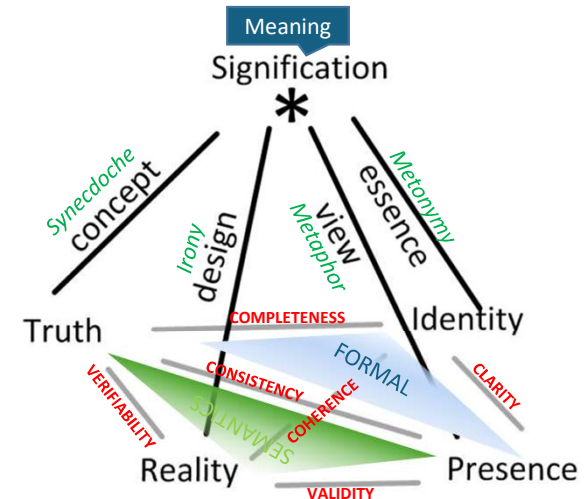
‘machine’, ‘organism’, ‘cultural/political’,
‘societal/environmental’ ‘interrelationships’



General Schemas Theory (Kent Palmer 2019):



Quadralectics



Present

Verification (Built the System Right)

“The purpose of the Verification process is to provide objective evidence that a system, system element, or artifact fulfills its specified requirements and characteristics.”

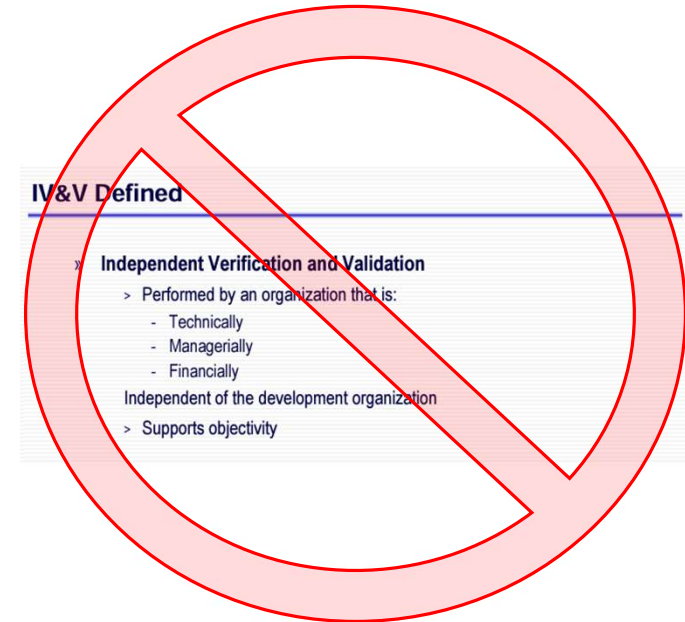
Validation (Built the Right System)

“The purpose of the Validation process is to provide objective evidence that the system, when in use, fulfills its business or mission objectives and stakeholder needs and requirements, achieving its intended use in its intended operational environment.”

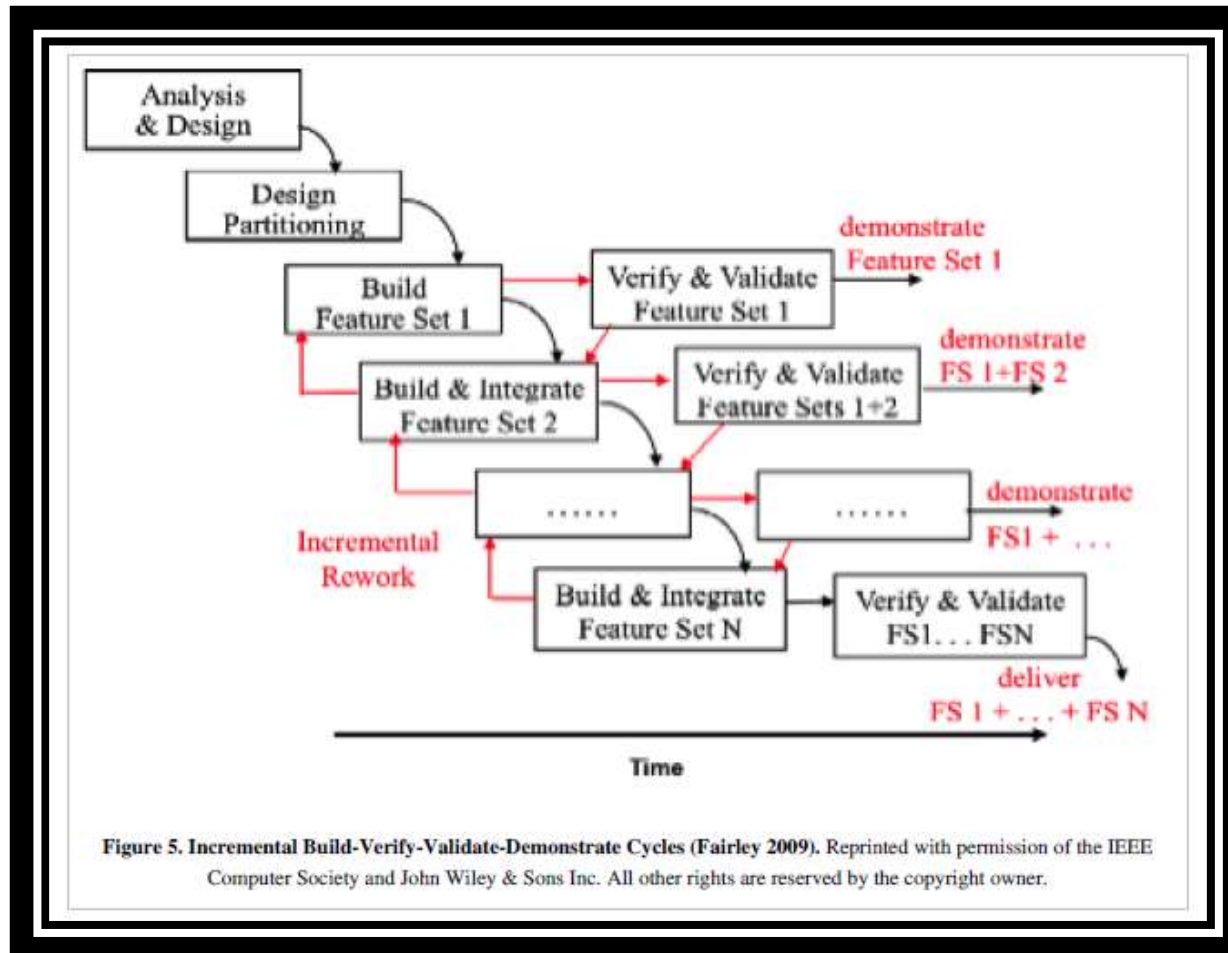
Integration (Building)

“The purpose of integration is to synthesize a set of system elements into a realized system that satisfies the system requirements.”

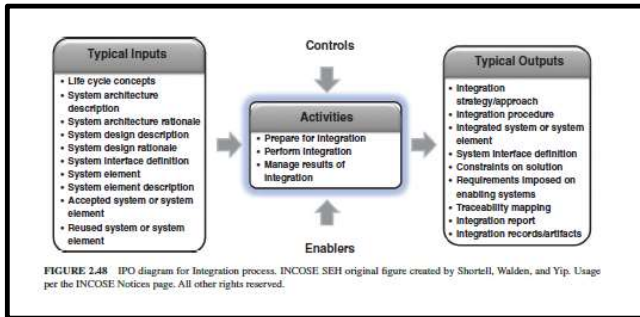
“Coupling Matrix and N-squared Diagram: One of the most basic methods to define the aggregates and the order of integration would be the use of N-Squared diagrams.” - Source: SEBOK V1.4 / sebokwiki.org



Source: INCOSE Handbook V5 Section 2.3.5 Technical Processes

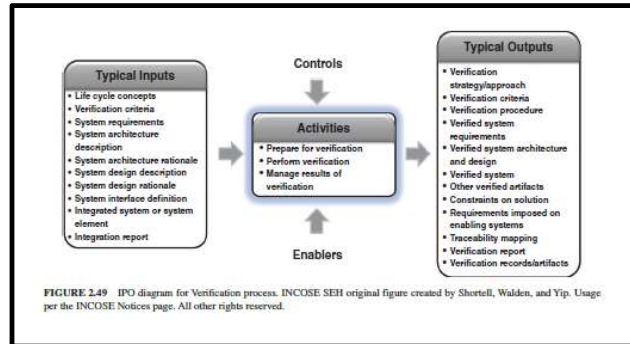


On Incremental Process for IV&V Between Classic and Agile Source: SEBOK V1.4 (see sebokwiki.org)



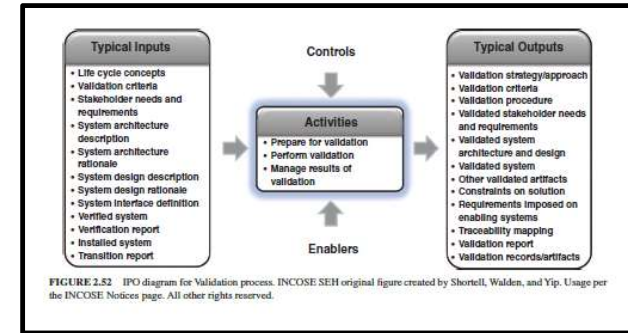
- I Life cycle concepts
- I System architecture description
- I System architecture rationale
- I System design description
- I System design rationale
- I System interface definition
- I System element
- I System element description

- O Integration strategy/approach
- O Integration procedure
- O Integrated system or system element
- O System interface definition
- O Constraints on solution
- O Requirements imposed on enabling systems
- O Traceability mapping
- O Integration report
- O Integration records/artifacts



- I Life cycle concepts
- I Verification criteria
- I System requirements
- I System architecture description
- I System architecture rationale
- I System design description
- I System design rationale
- I System interface definition
- I Integrated system or system element
- I Integration report

- O Verification strategy/approach
- O Verification criteria
- O Verification procedure
- O Verified system requirements
- O Verified system architecture and design
- O Verified system
- O Other verified artifacts
- O Constraints on solution
- O Requirements imposed on enabling systems
- O Traceability mapping
- O Verification report
- O Verification records/artifacts



- I Life cycle concepts
- I Validation criteria
- I Stakeholder needs and requirements
- I System architecture description
- I System architecture rationale
- I System design description
- I System design rationale
- I System interface definition
- I Verified system
- I Verification report
- I Installed system
- I Transition report

- O Validation strategy/approach
- O Validation criteria
- O Validation procedure
- O Validated stakeholder needs and requirements
- O Validated system architecture and design
- O Validated system
- O Other validated artifacts
- O Constraints on solution
- O Requirements imposed on enabling systems
- O Traceability mapping
- O Validation report
- O Validation records/artifacts

	EXT	BMA	SNRD	SRD	AD	DD	SA	IMPL	INT	VER	TRAN	VAL	OPER	MAINT	DISP	PF	PAC	DM	RM	CM	INFOM	MEAS	QA	ACC	SUP	LCMM	INFRAM	PM	HRM	QM	KM	TLR	
EXT	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
BMA	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
SNRD	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
SRD	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
AD	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
DD	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
SA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1
IMPL	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1
INT	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1
VER	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1
TRAN	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1
VAL	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	1
OPER	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1
MAINT	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1
DISP	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	1
PF	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1
PAC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
DM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1
RM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1
CM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1
INFOM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1
MEAS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
QA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
ACC	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
SUP	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
LCMM	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
INFRAM	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
PM	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
HRM	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
QM	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
KM	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
TLR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Green Circle indicates that the link actually occurred in the Input/Output Process Diagrams found throughout the INCOSE Handbook versus those listed (rather generously) in the Published N-Squared in the Appendix

Some Practical Considerations for Integration, Verification, and Validation

1. How many subsystem and system tolerance variances should you “insert” into the Integration Plan?
2. How many Verification and Validation tests should you perform?
3. Should you include White Box and Black Box / Normal Operation and Personas / Faulted-Abnormal Operations and Shadow Personas?
4. How much credit can you take at higher levels for subsystem tests at lower level?
5. How much credit can you provide the tools used for building subsystems (e.g. CAD tools, Compilers, etc.)
6. How does qualification and acceptance testing relate to V&V?
7. How do inspections performed as part of manufacturing relate to verification? (Is it essentially two step verification...you verify the design to the requirements and then the inspection verifies the item to the design?)

Note: Thales has a title **IVVQ Engineer** separate from Systems Engineer: “As an *Integration, Verification, Validation and Qualification (IVVQ) Engineer* you will focus on the ‘right hand side of the V’ to deliver solutions to customers in our Civil and Military domains.” (thalesgroup.com)

Future

One View of a V&V Roadmap...

- MBSE automated Code Generation (MDA Model Drive Architecture, [Code Gen](#))
- MBSE automated Rapid Prototypes (3D Print, Code, Simulations, AR)
- Design of Experiments to reduce Test Samples
- PBSE [Utilizing MBSE Patterns to Accelerate System Verification](#)
- [Bayesian Networks / Risk Distributions](#) vs. Red/Yellow/Green
- AI-Generated Requirements and Test Cases (e.g. <https://tracespace.app>)
- [Schema Validation](#) (Kent Palmer); [Critical Sociotechnical Methods](#) (Michael C. Jackson)
 - Highly Complex Systems with Emergent and Reflexive Learning Properties
- [Quantum Computing Algorithms](#) (e.g. Topological Quantum Codes)
- Using Appropriate [Topologies and Manifolds to Reduce Tests Cases](#)