

Verification & Validation with Model-Based Design

Lyle Shipton
Application Engineer
MathWorks
Plano, TX

Background

- University of Illinois at Urbana-Champaign
 - B.S, M.S. Aerospace Engineering
- SpaceX Rocket Development Facility
 - Test Engineer
 - Lead Engineer, Integration & Test
- Eaton Aerospace, Fuel and Motion Controls
 - Lead Aerospace Systems Engineer
- MathWorks, Application Engineering Group
 - Lead Engineer, Aeronautical applications



MathWorks at a Glance

- Privately held
- 4000 employees worldwide
- More than 3 million users in 180+ countries



● Office locations

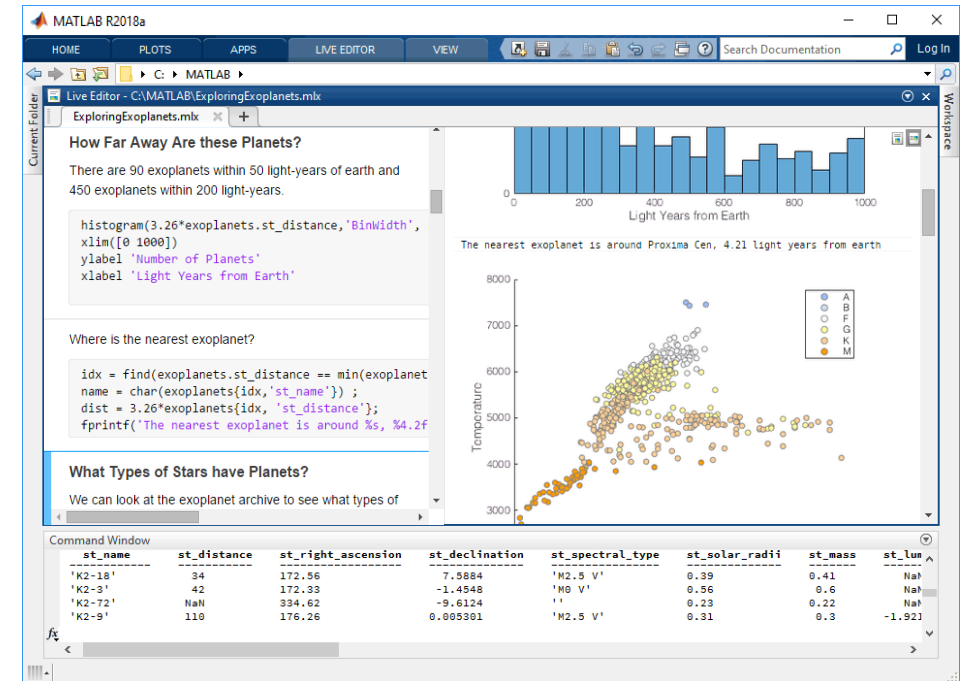
● Distributors serving 16 countries

Core MathWorks Products

MATLAB®

Math. Graphics. Programming.

- Designed for engineers and scientists
- Professionally developed, tested, and documented
- Toolboxes for:
 - Machine learning, data analytics, deep learning, image processing and computer vision, signal processing and communications, computational finance, robotics and control systems
- Interactive apps that automatically generate programs
- Easily scales to clusters, GPUs, and clouds
- Direct deployment to production enterprise applications
- Automatic conversion to embeddable C and CUDA code
- Integrates with Simulink to support Model-Based Design



Core MathWorks Products

SIMULINK®

Simulation and Model-Based Design

Model and simulate your system

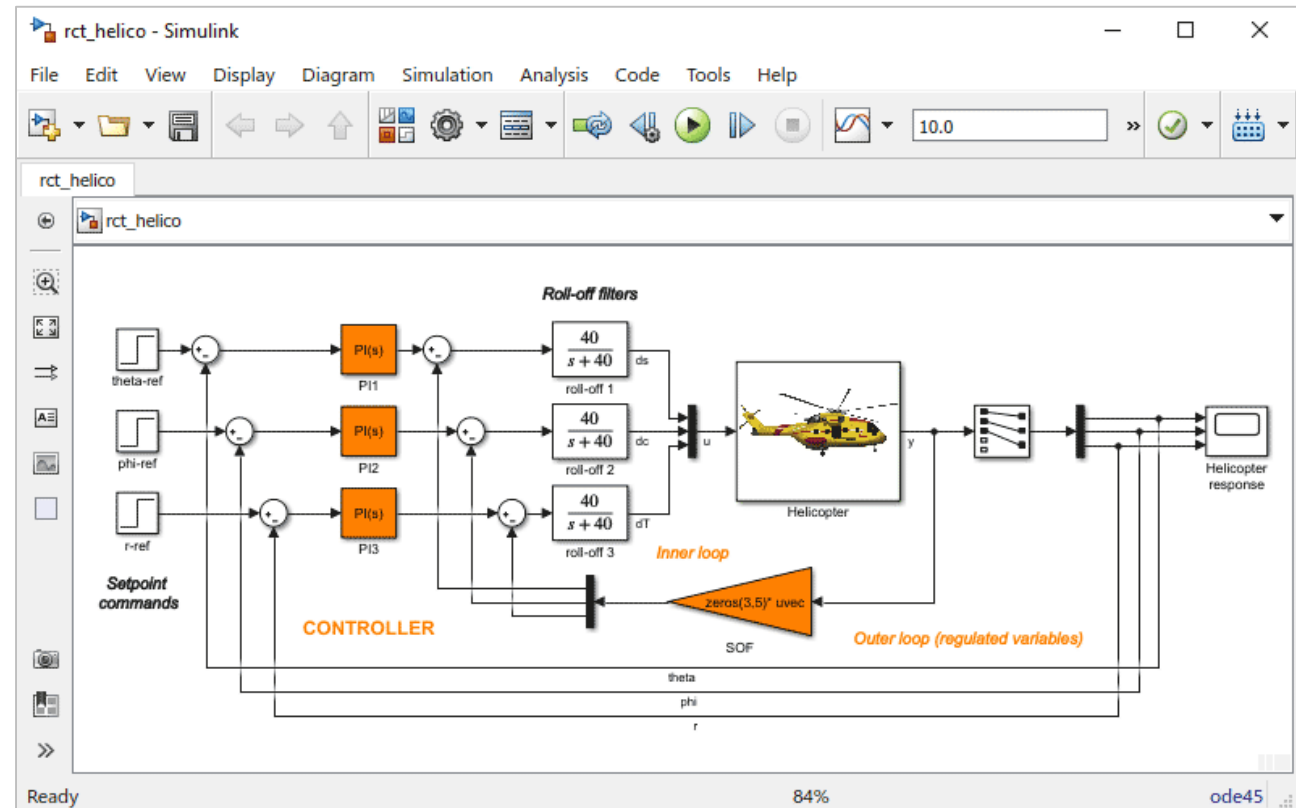
- Use one multi-domain environment
- Model the system under test and the plant
- Simulate how all parts of the system behave

Test early and often

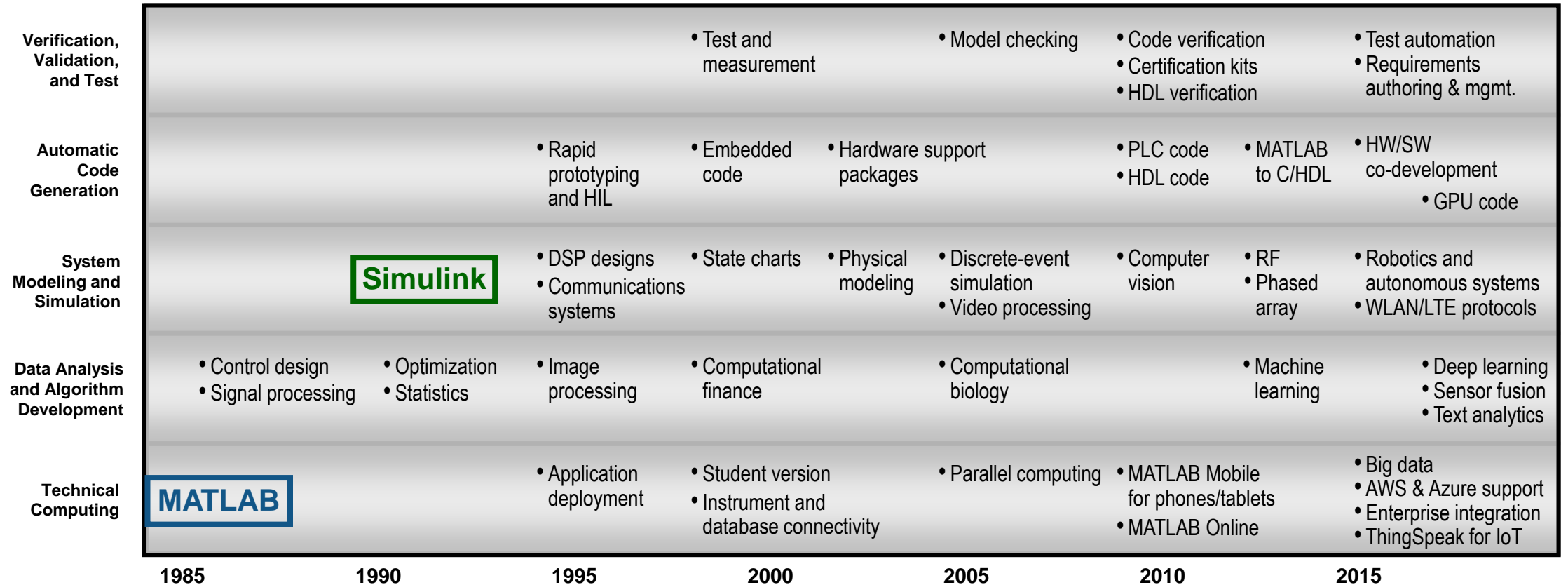
- Test your system under all conditions
- Validate your design with real-time testing
- Trace from requirements to design to code

Automatically generate code

- Generate production-quality C and HDL code
- Deploy directly to embedded processors or FPGA's/ASIC's

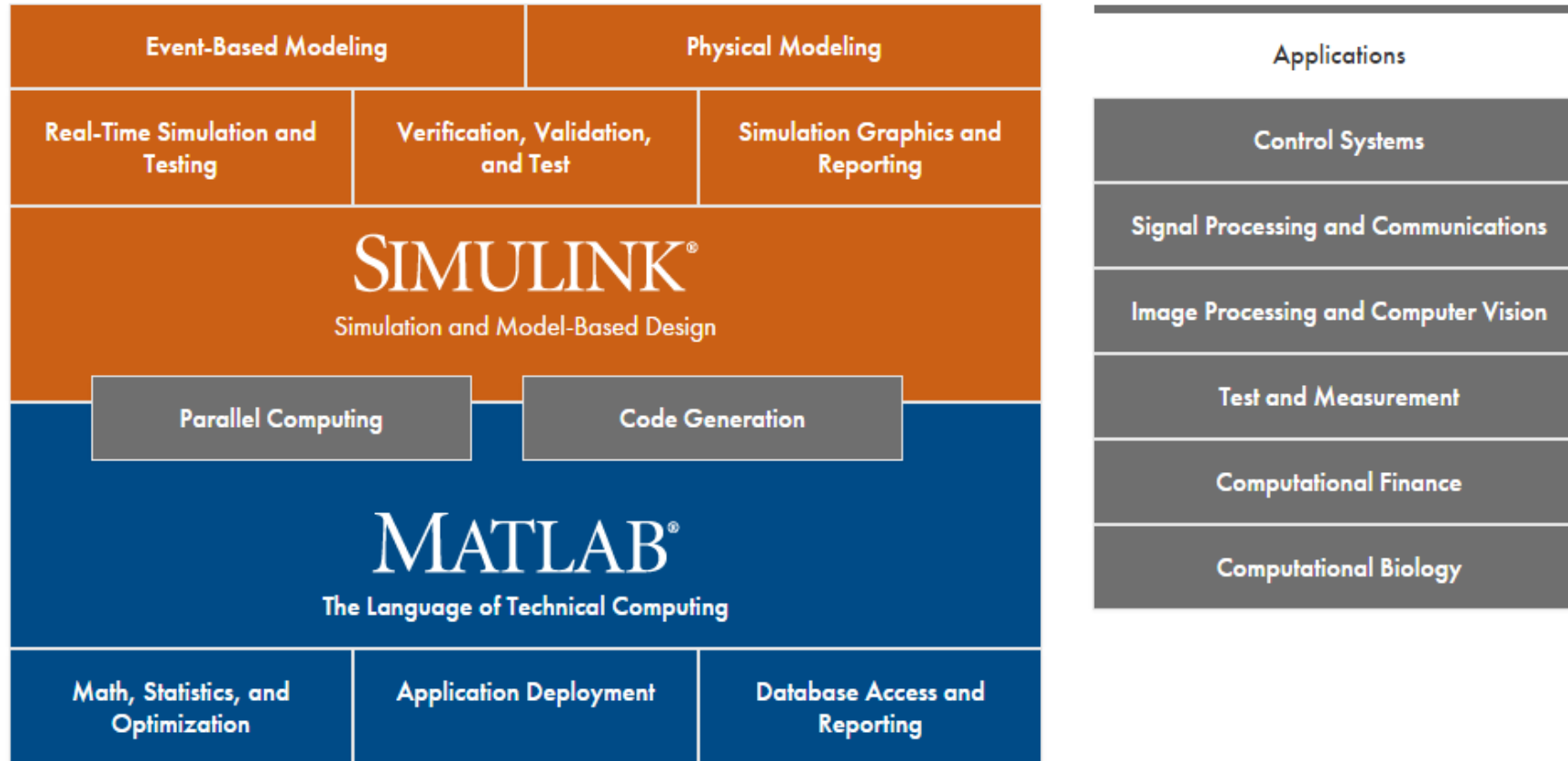


Key capabilities for engineers and scientists

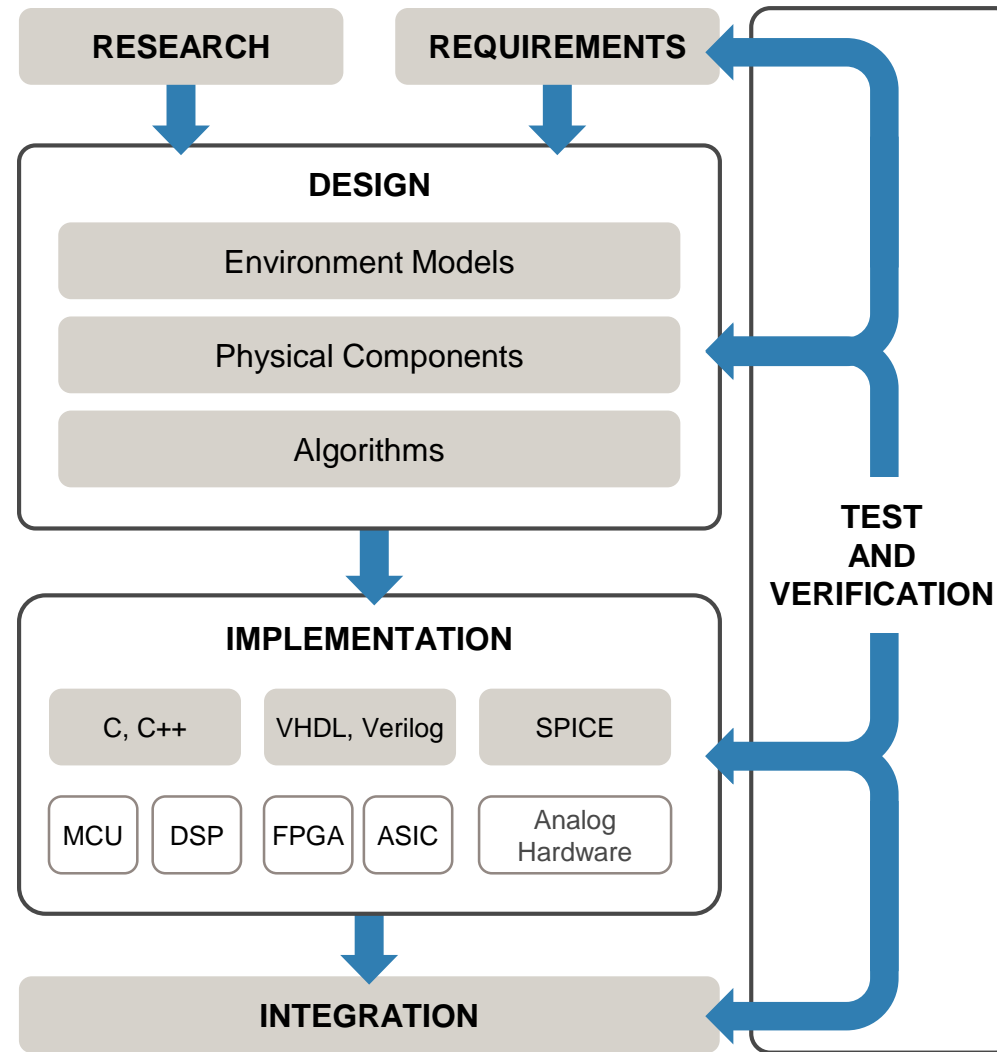


MathWorks
founded
in 1984

MathWorks Product Overview



Model-Based Design Workflow



Key Takeaways

1. Find bugs early, develop high quality systems
2. Replace manual verification tasks with workflow automation
3. Learn about reference workflow that conforms to safety standards

“Reduce costs and project risk through early verification, shorten time to market on a certified system, and deliver high-quality production code that was first-time right” Michael Schwarz, ITK Engineering

System Requirements

maximum machine velocity, left track
maximum machine acceleration, left track
maximum machine jolt, left track
motor speed for 50% rise time, left track
95% rise time, left track
motor speed for 95% rise time, left track
95% rise time, left track
maximum machine velocity, right track
maximum machine acceleration, right track
maximum machine jolt, right track
motor speed for 50% rise time, right track

High Level Design

Detailed Design

Coding

Integration Testing

Unit Testing

Verified & Validated System



Safety of Electronic Systems

- Critical functionality in industries such as Aerospace, Automotive, and Industrial Automation
- Real-time operation
 - Compute time lag cannot be tolerated
- Predictable behavior
 - No unintended functionality
- Must be robust
 - Program crash or reboot not allowed

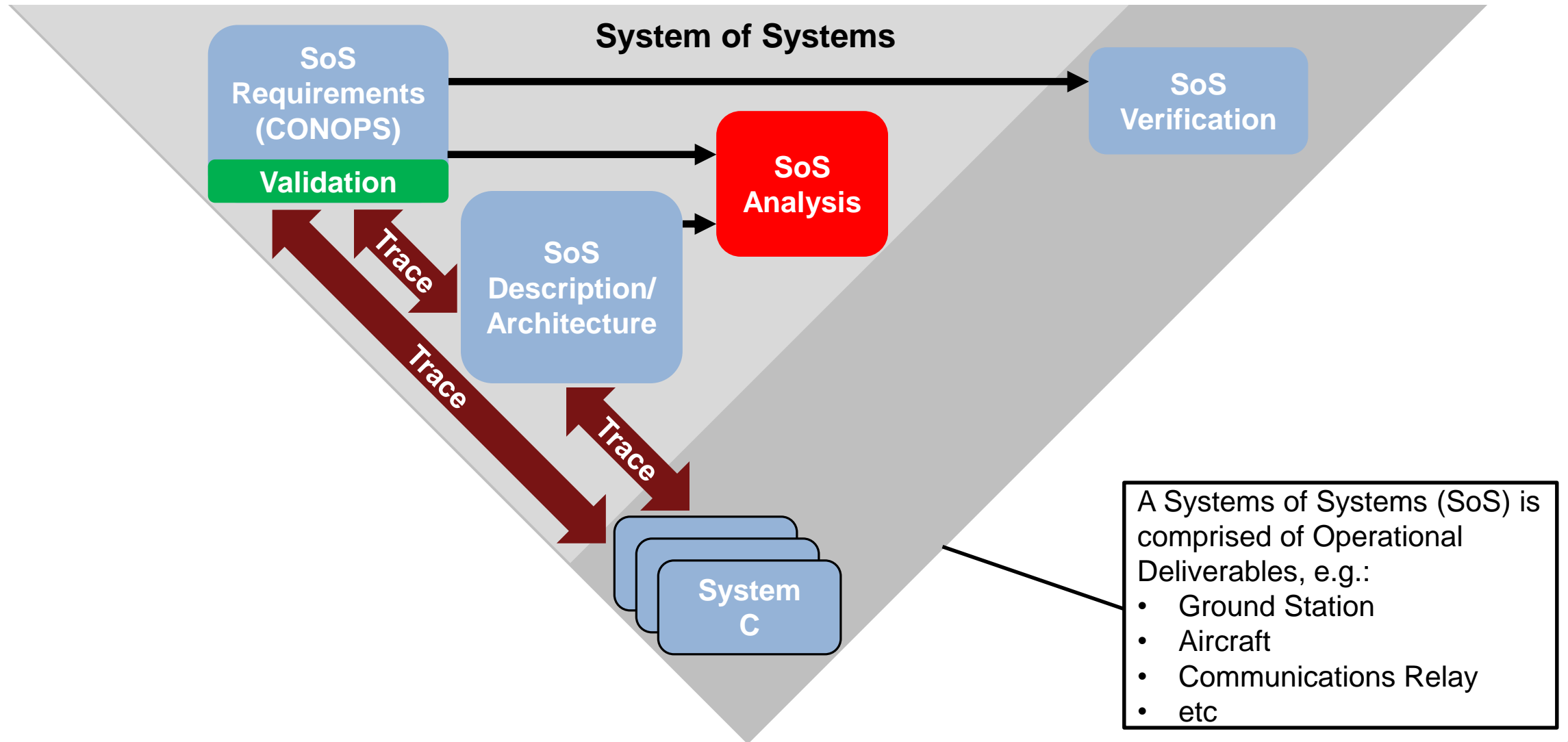


Role of Certification Standards

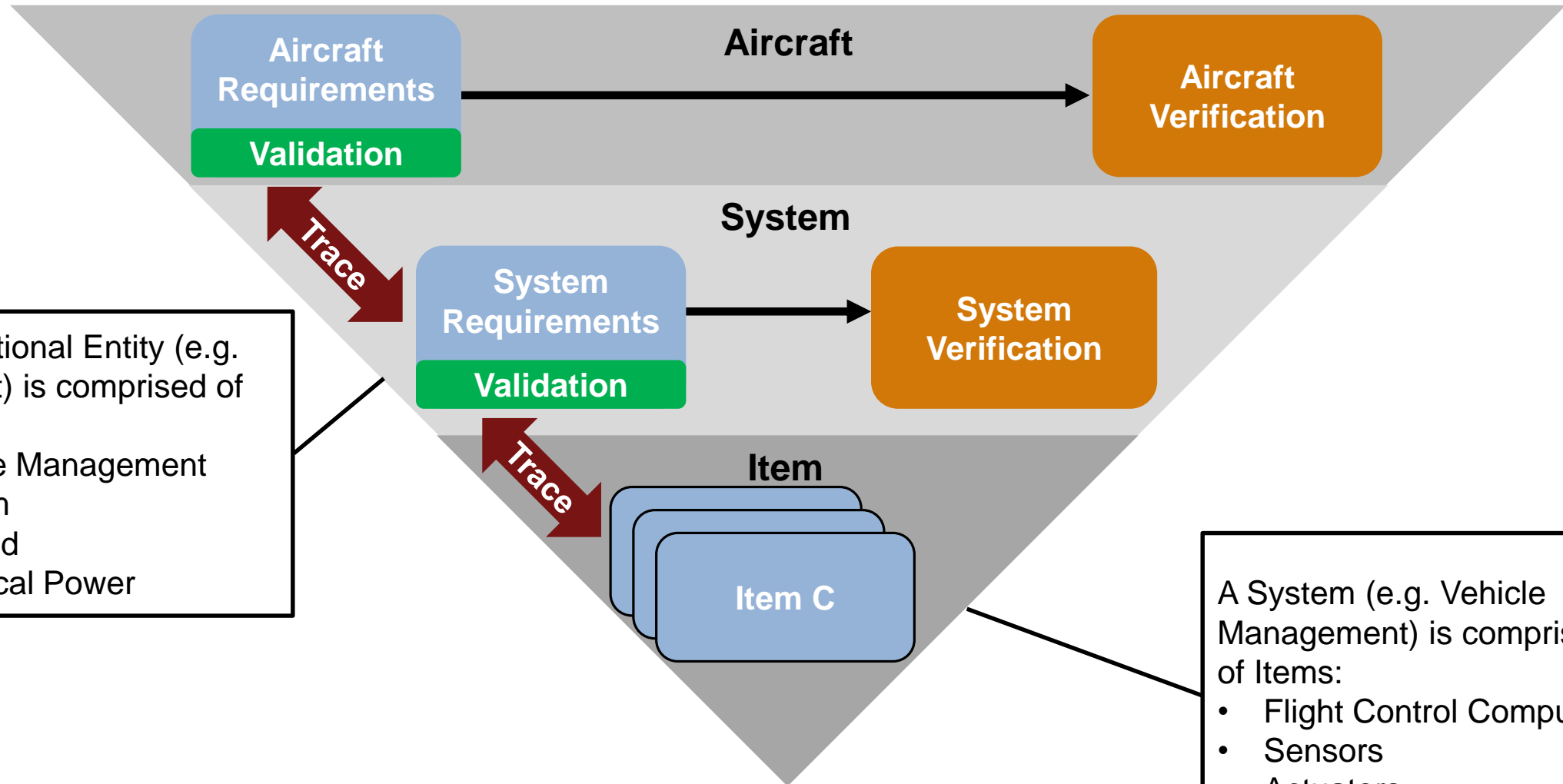
- DO-178 (Avionics)
 - Guidelines for the safety of software in certain airborne systems
 - Level A to E (most critical to least)
 - Verification activities include review of requirements and code, testing of software, code coverage
- ISO 26262 (Automotive)
 - Defines functional safety for automotive electronic systems
 - Automotive Safety Integrity Level ASIL QM, A to D (least to most; derived from severity, controllability, probability)
 - ISO 26262-6 pertains to software development, verification, and validation
- IEC 61508 (Industrial Automation & Machinery)
 - General functional safety standard, originally for process control industry
 - Safety Integrity Level SIL 1 to 4 (least to most; derived from exposure to demand needs and probability of failure)
 - Defines the software requirements and lifecycle for software, that includes validation and verification

Reference Verification and Validation Workflow

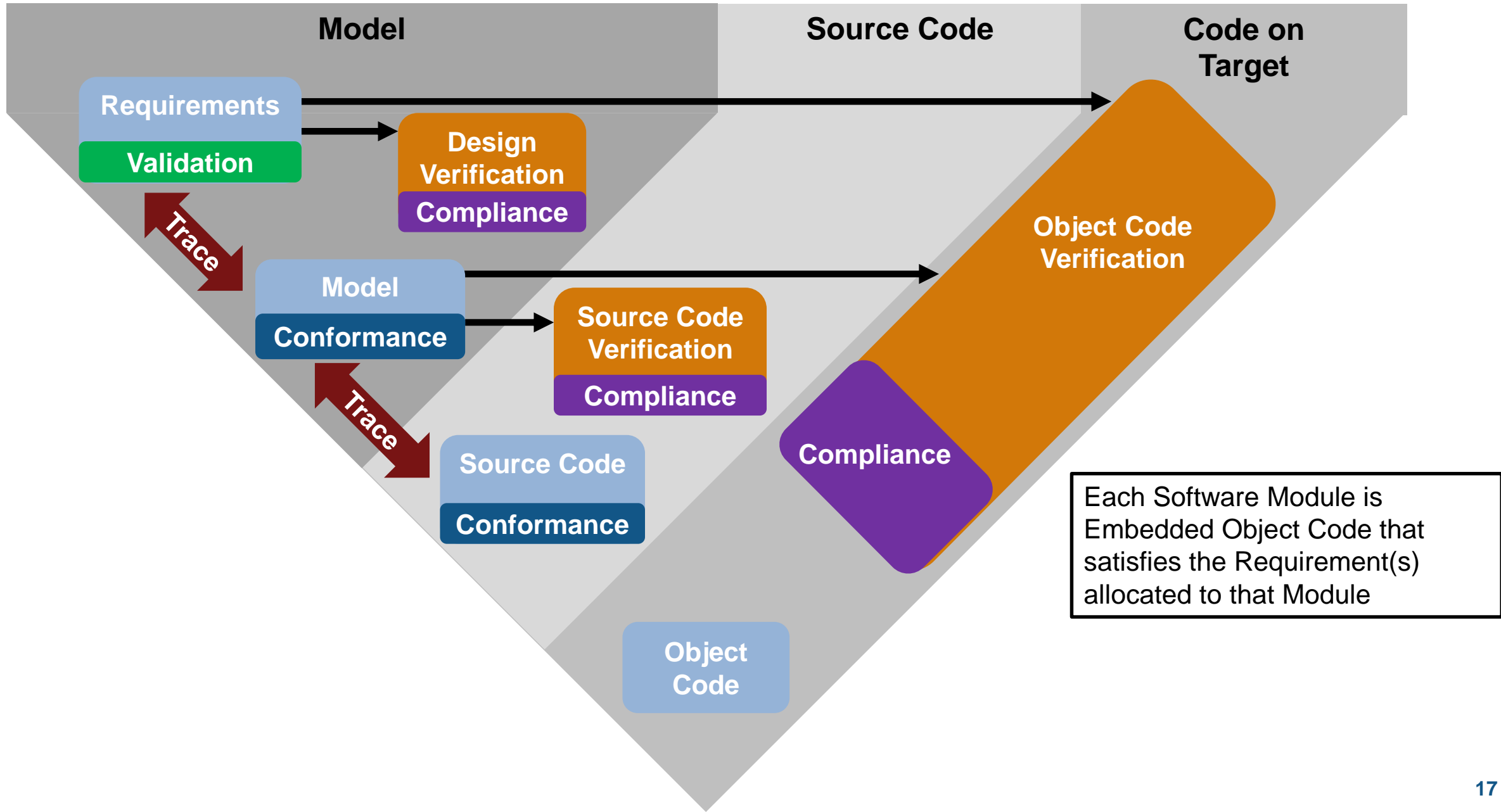
Development Process and Workflow



Development Process and Workflow

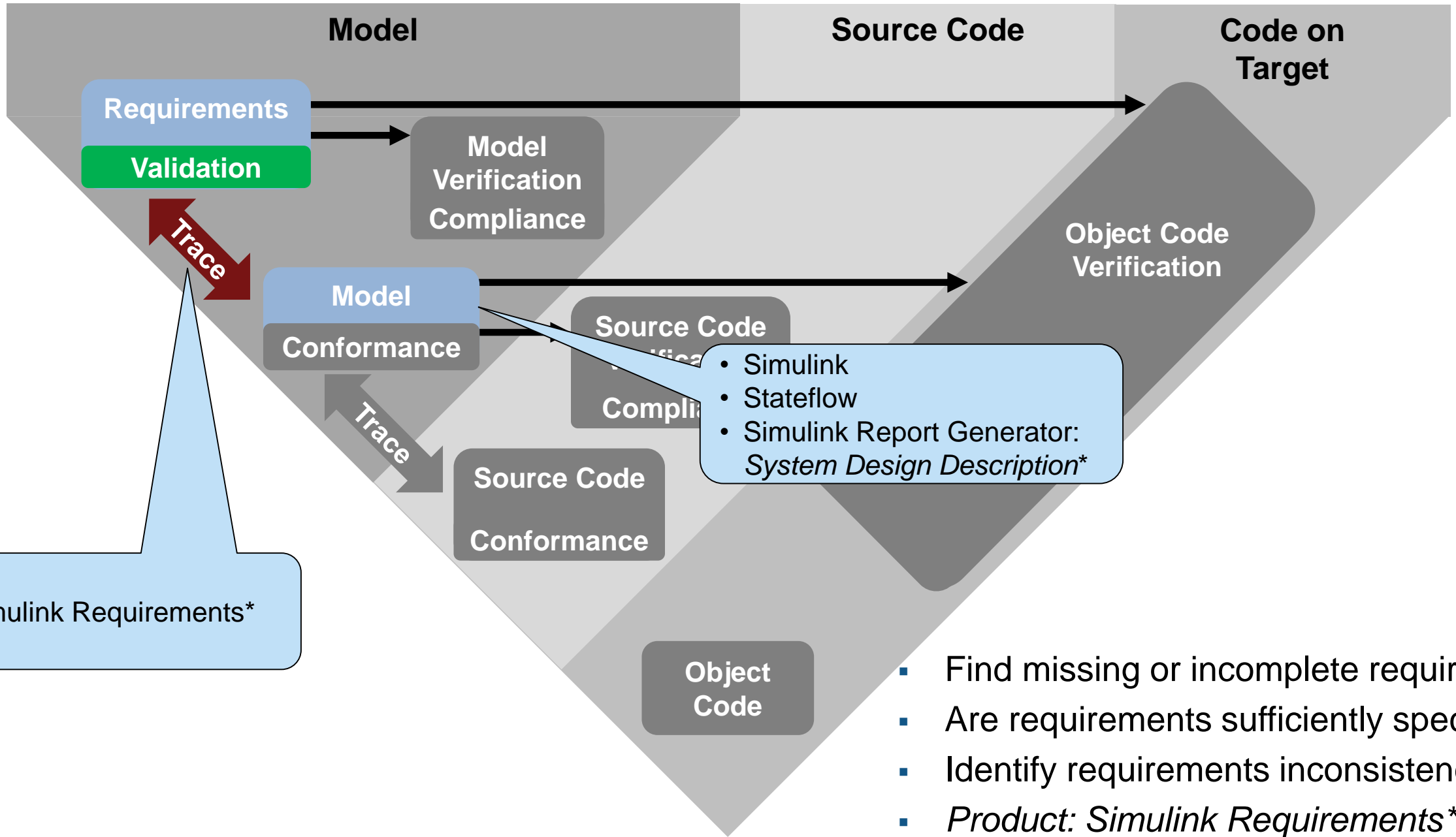


Development Process and Workflow



Verification and Validation Tasks and Activities

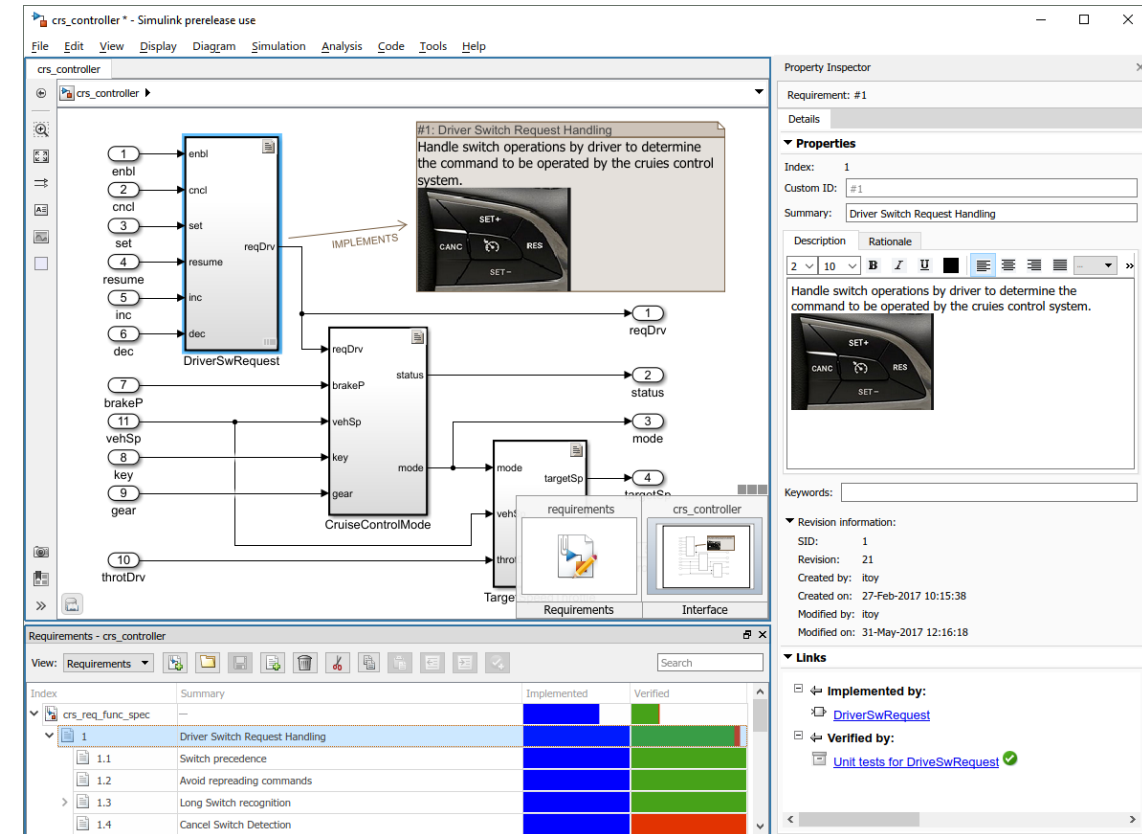
Verification and Validation Tasks and Activities



Simulink Requirements

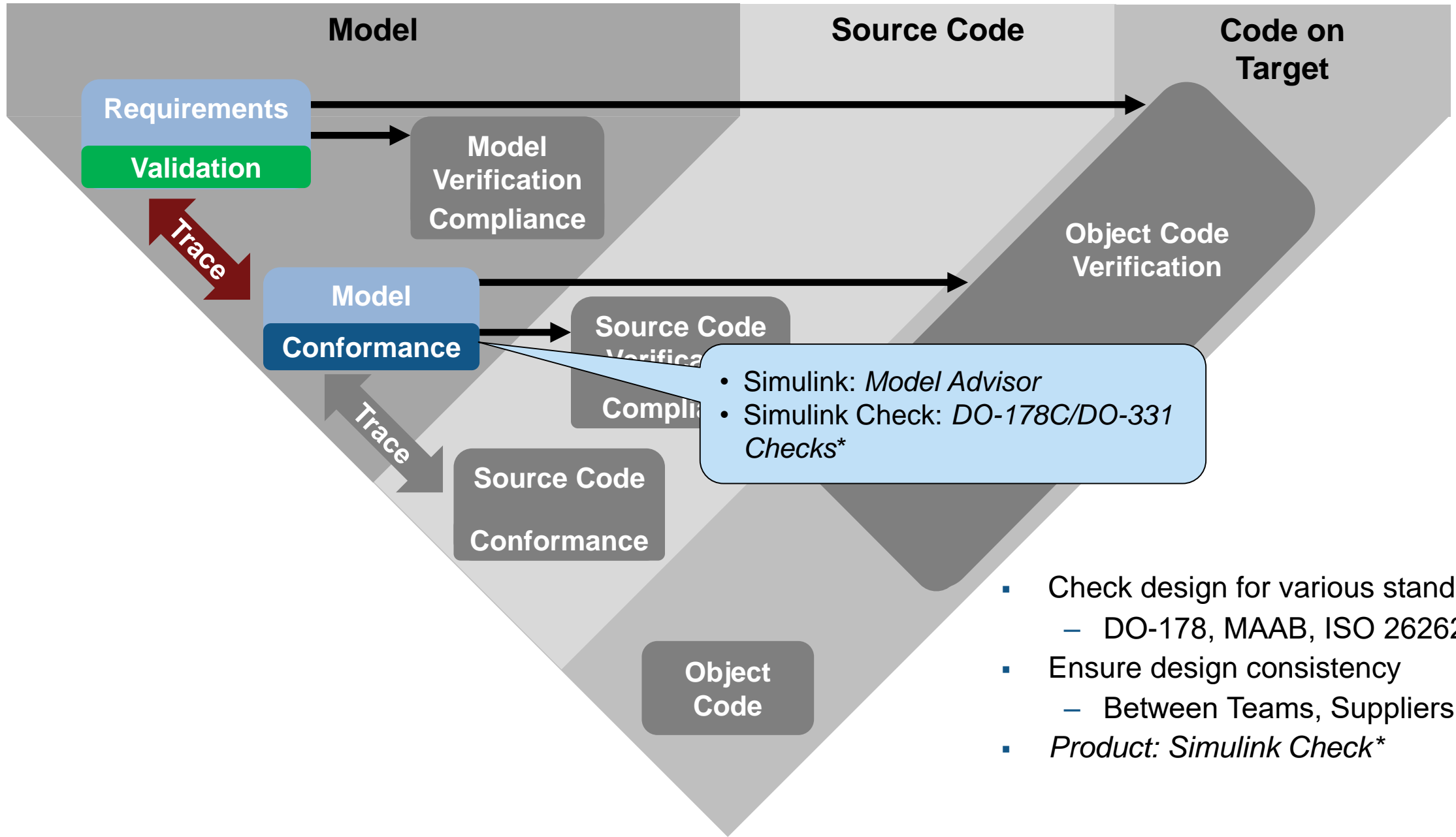
Work with requirements and design together

- Author, edit and organize requirements
- View and link requirements within the Simulink graphical editor
- Track status and manage requirement changes
- Trace requirements to models, generated code, and test cases

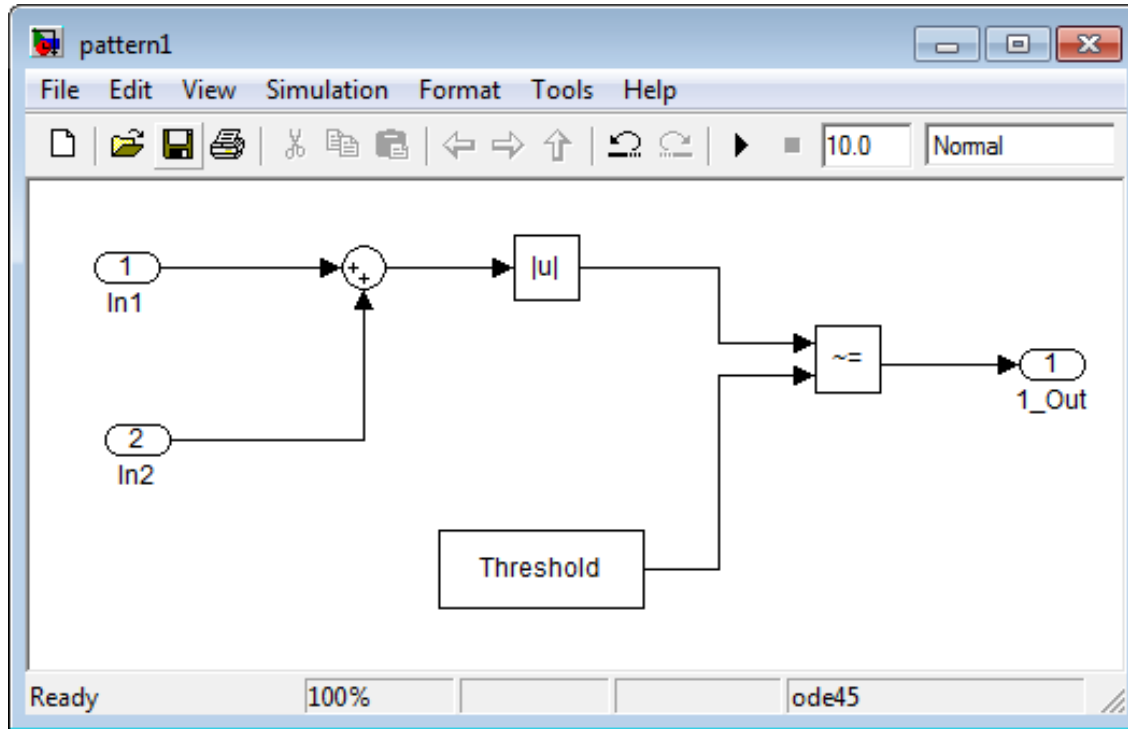


Requirements Perspective

Verification and Validation Tasks and Activities



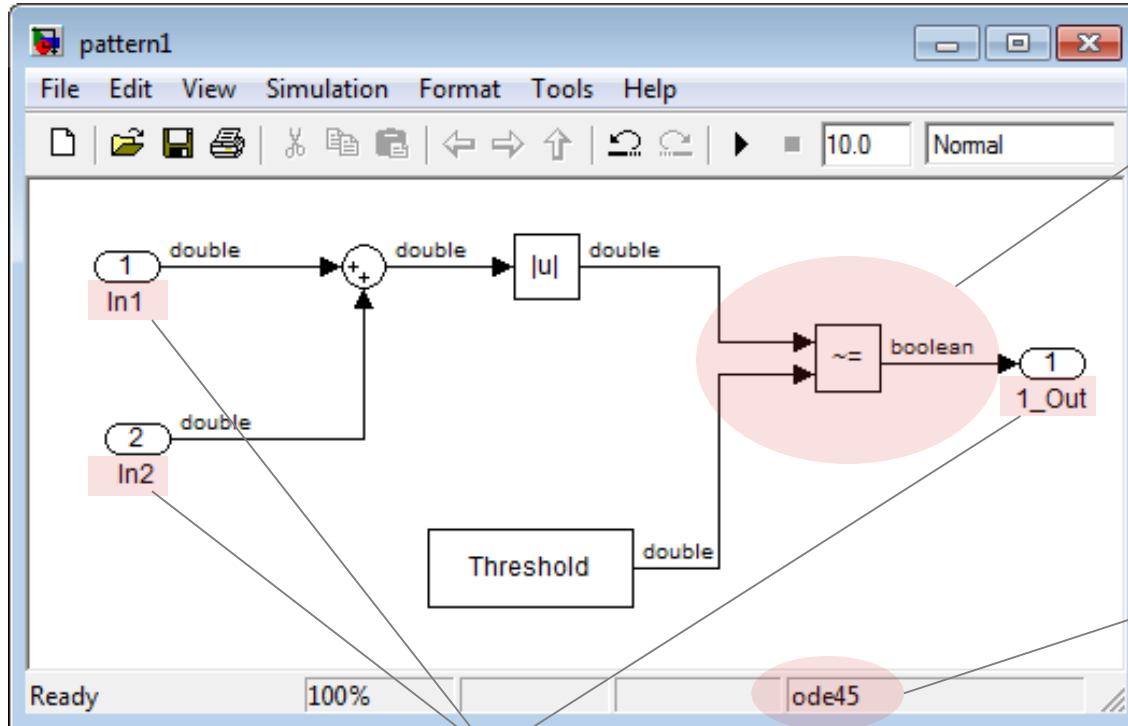
Example



Is there a potential error in this model? It depends...

Example

How about now?



When generating code:

- Floating-point precision issues may lead to incorrect comparison results

Is this a production model?

- Implementation requires a fixed-step, discrete solver

- Ports do not follow established naming conventions

Simulink Check

Automate verification and correct models to improve design

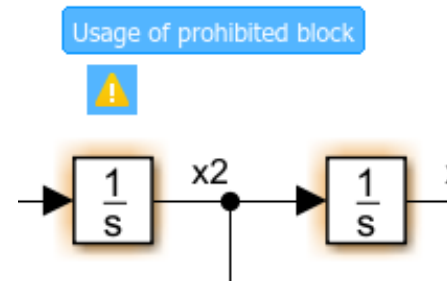
Standards & Guidelines Checks

- Automate compliance to standards
- Create custom checks

- ✓ Modeling Standards for DO-178C/DO-331
- ✓ Modeling Standards for EN 50128
- ✓ Modeling Standards for IEC 61508
- ✓ Modeling Standards for IEC 62304
- ✓ Modeling Standards for ISO 26262
- ✓ Modeling Standards for MAAB
- ✓ Modeling Standards for MISRA C:2012
- ✓ Modeling Standards for Secure Coding (CERT C,

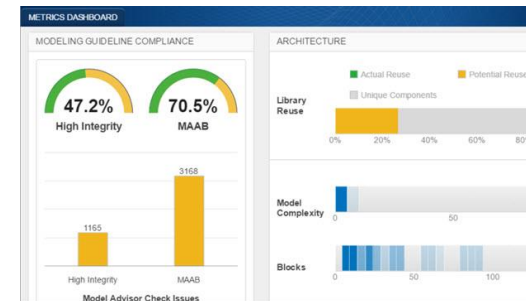
Edit Time Checking

- Find and fix compliance issues while you design



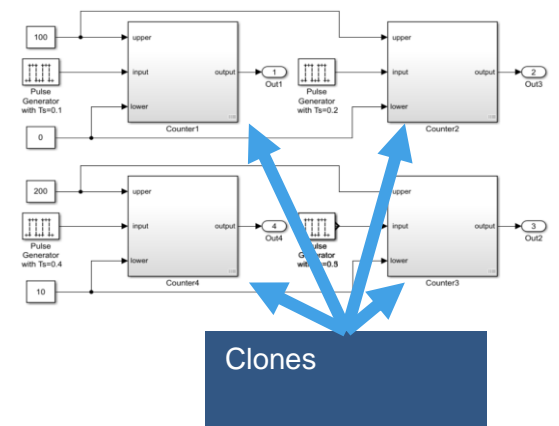
Model Metrics

- Analyze your model for complexity, size, reusability
- Assess design quality

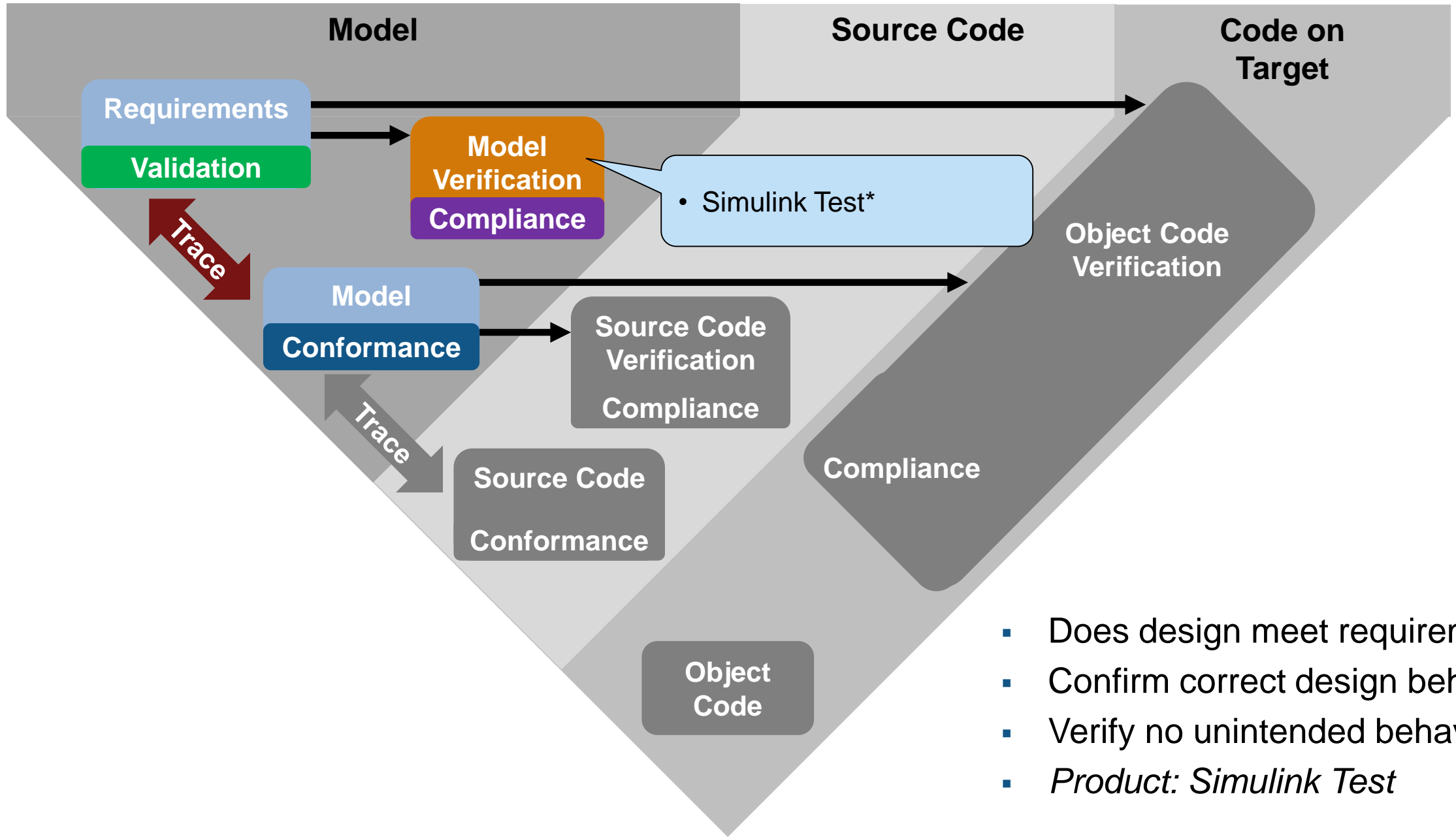


Model Refactoring

- Find clones and modeling patterns.
- Refactor to improve maintainability



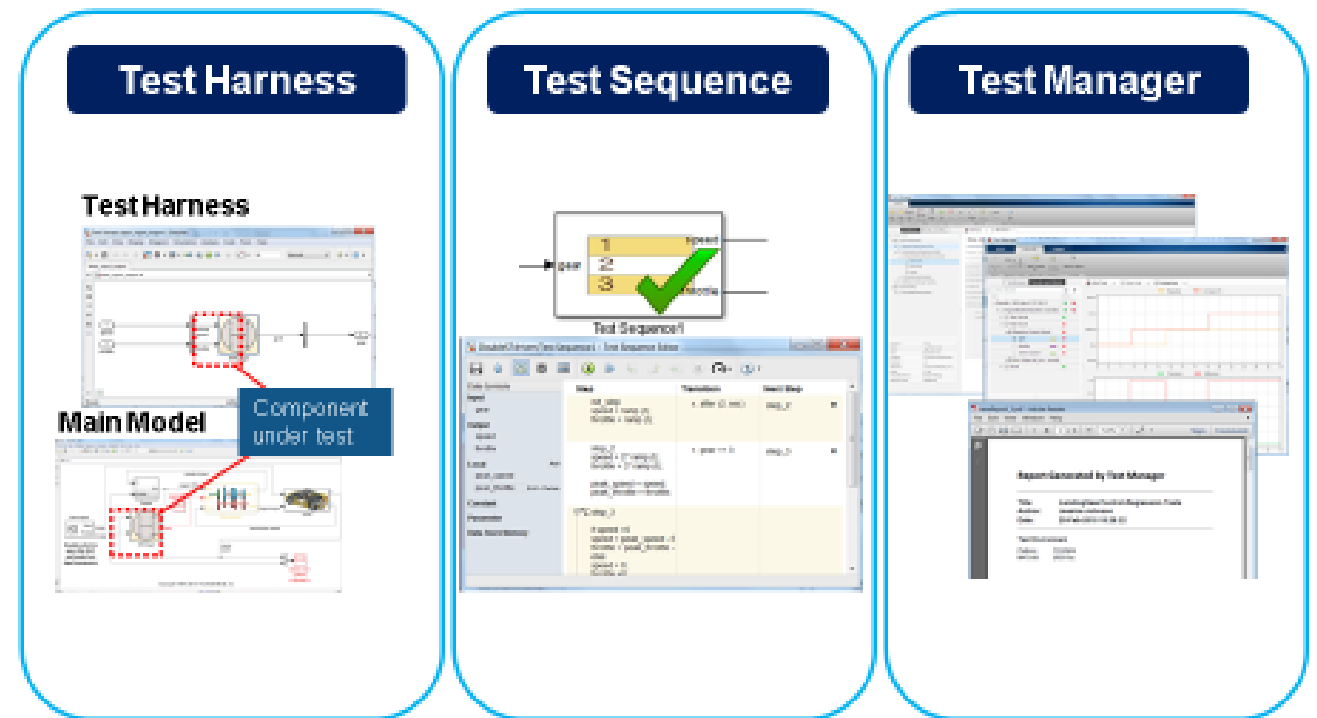
Verification and Validation Tasks and Activities



- Does design meet requirements
- Confirm correct design behavior
- Verify no unintended behavior
- *Product: Simulink Test*

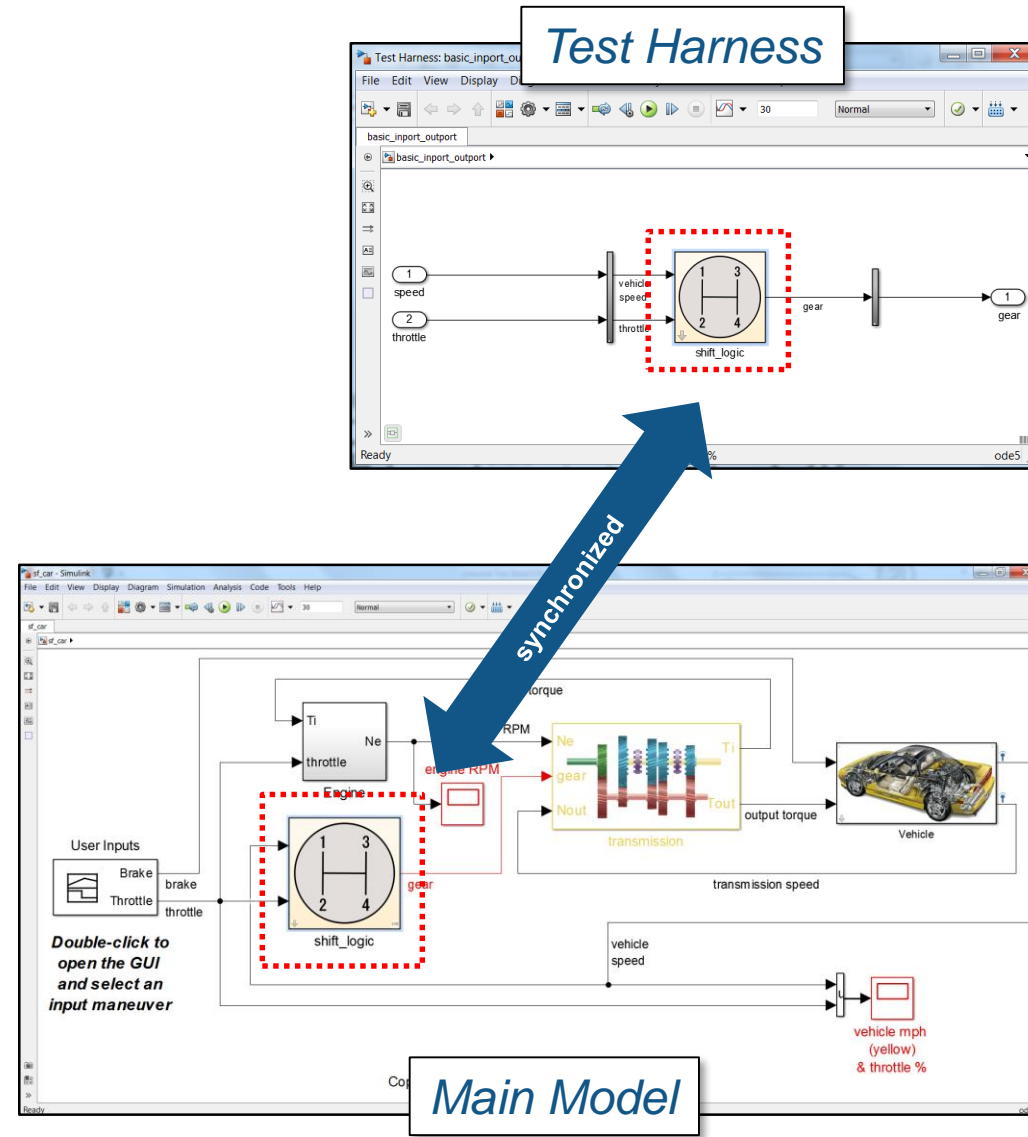
Functional Testing Process

- Author test-cases that are derived from requirements
 - Use test harness to isolate component under test
 - Test Sequence to create complex test scenarios
- Manage tests, execution, results
 - Re-use tests for regression
 - Automate in Continuous Integration systems such as Jenkins



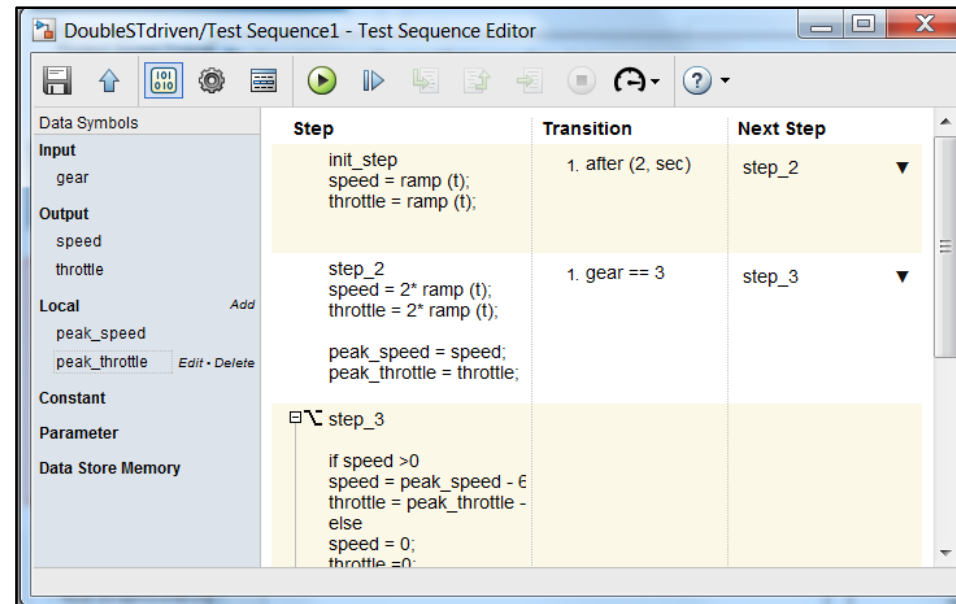
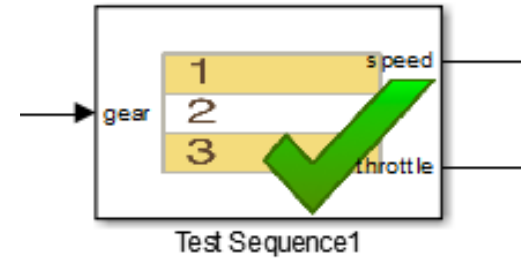
Test Harness

- ✓ Harnesses contained in the model file or external
- ✓ Build harness at unit (subsystem) or system level
- ✓ Synchronized test environment (harness \leftrightarrow model)
- ✓ Enables unit testing without requiring new model
- ✓ Configure harness input and output blocks
- ✓ Supports SIL, PIL, HIL



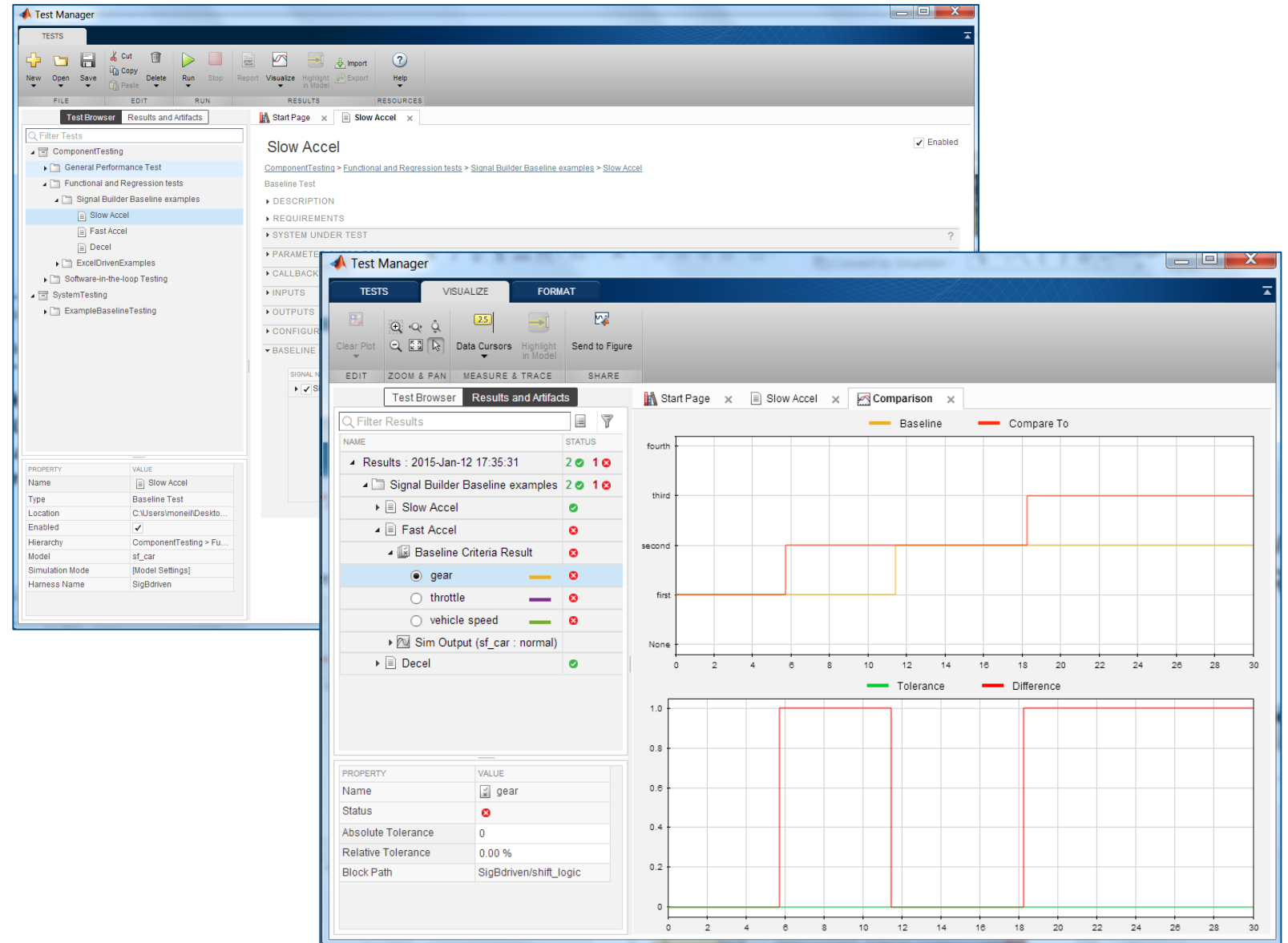
Test Sequence/Assessment Block

- ✓ Reactive and/or time based test cases
- ✓ Easier translation of test procedures
- ✓ Built on top of Stateflow with extensions for testing (SF license not required)
- ✓ Subset of MATLAB language
- ✓ Steps are temporal or logic-based
- ✓ Create complex test inputs and assessments
- ✓ Supports debugging (breakpoints)

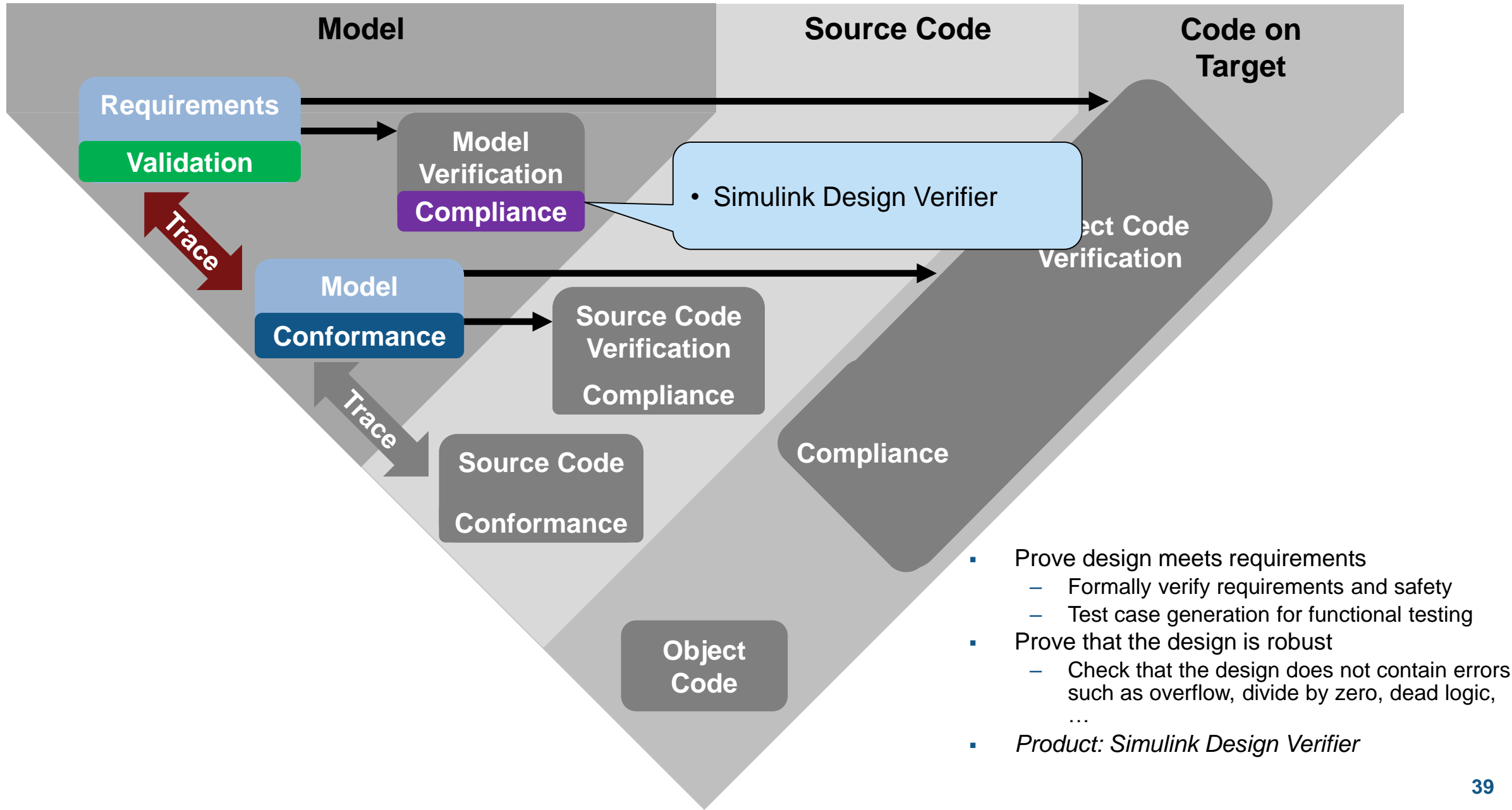


Test Manager

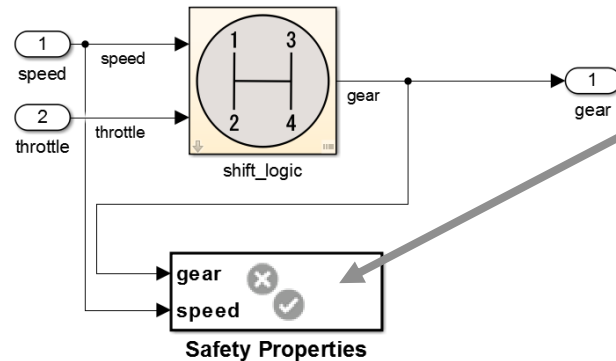
- ✓ Create test cases
- ✓ Group into suites and test files
- ✓ Execute individual or batch
- ✓ View result summary
- ✓ Analyze results
- ✓ Archive, export, report



Verification and Validation Tasks and Activities

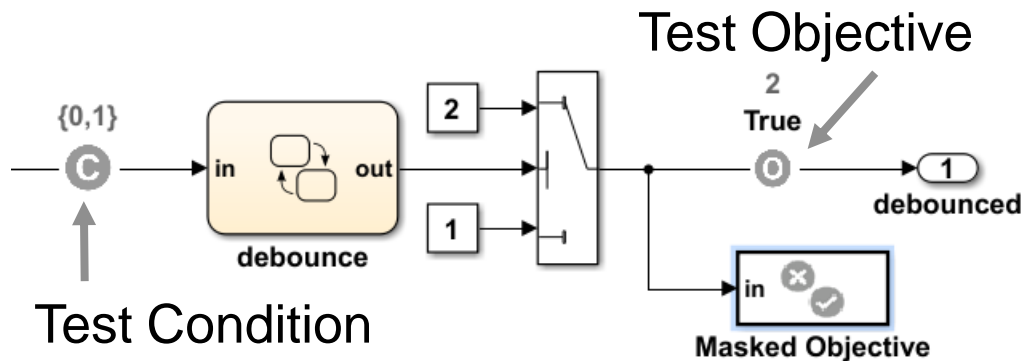


Formal Verification with Simulink Design Verifier



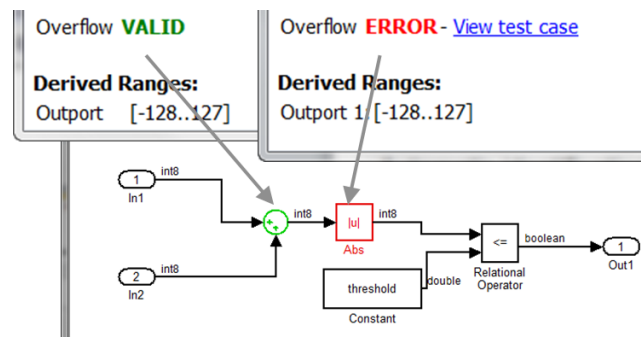
Checks that design meets requirements

- Gear 2 *always* engages when $\text{speed} \geq 5$ and ≤ 25
- Gear 2 *never* engages when $\text{speed} < 5$ or > 25



Automatically generate functional test case

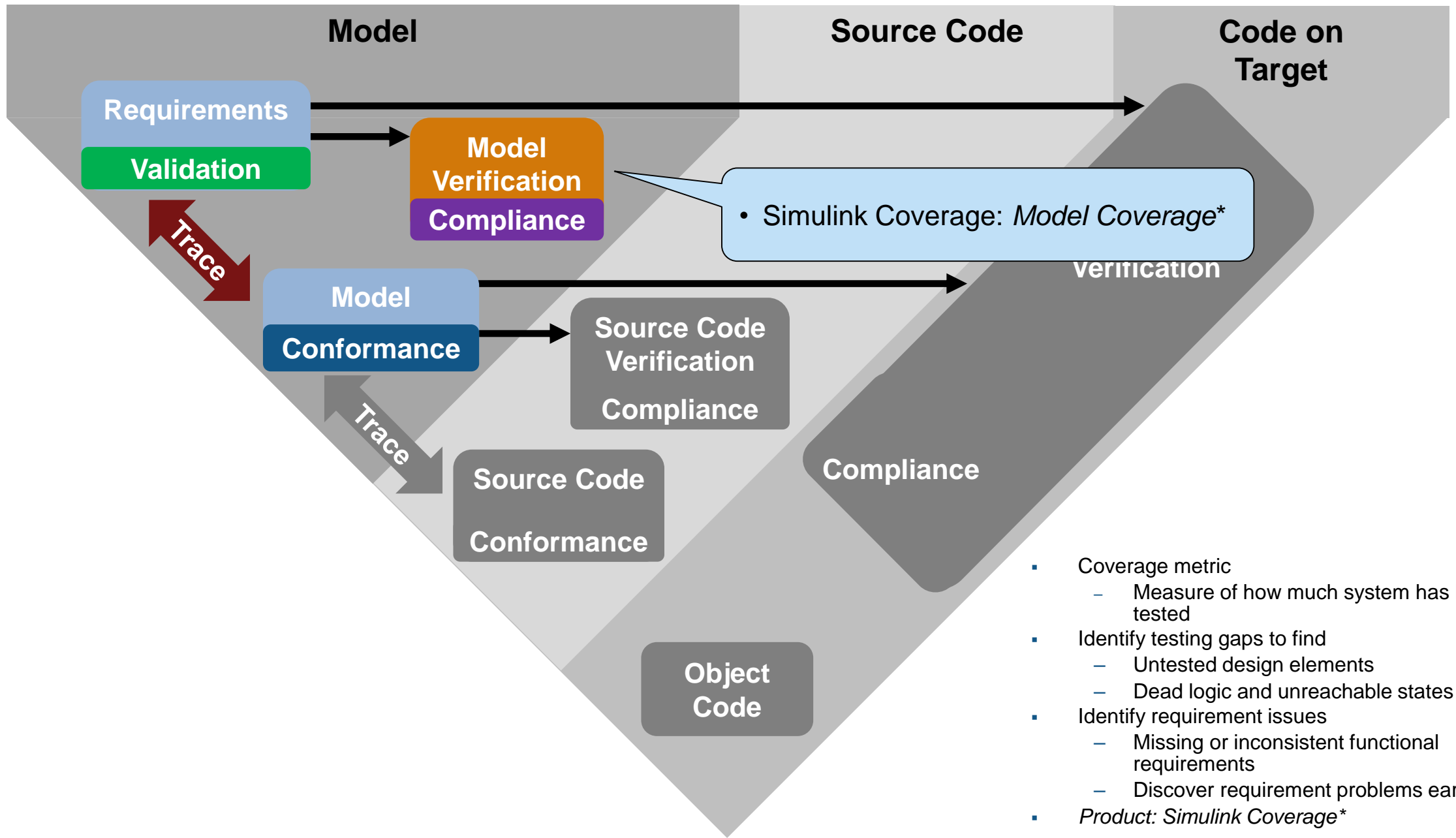
- Custom objectives signals must satisfy in tests
- Constraints on signal values for test generator



Detect overflows, divide by zero, and other robustness errors

- Proven that overflow does NOT occur
- Proven that overflow DOES occur

Verification Task

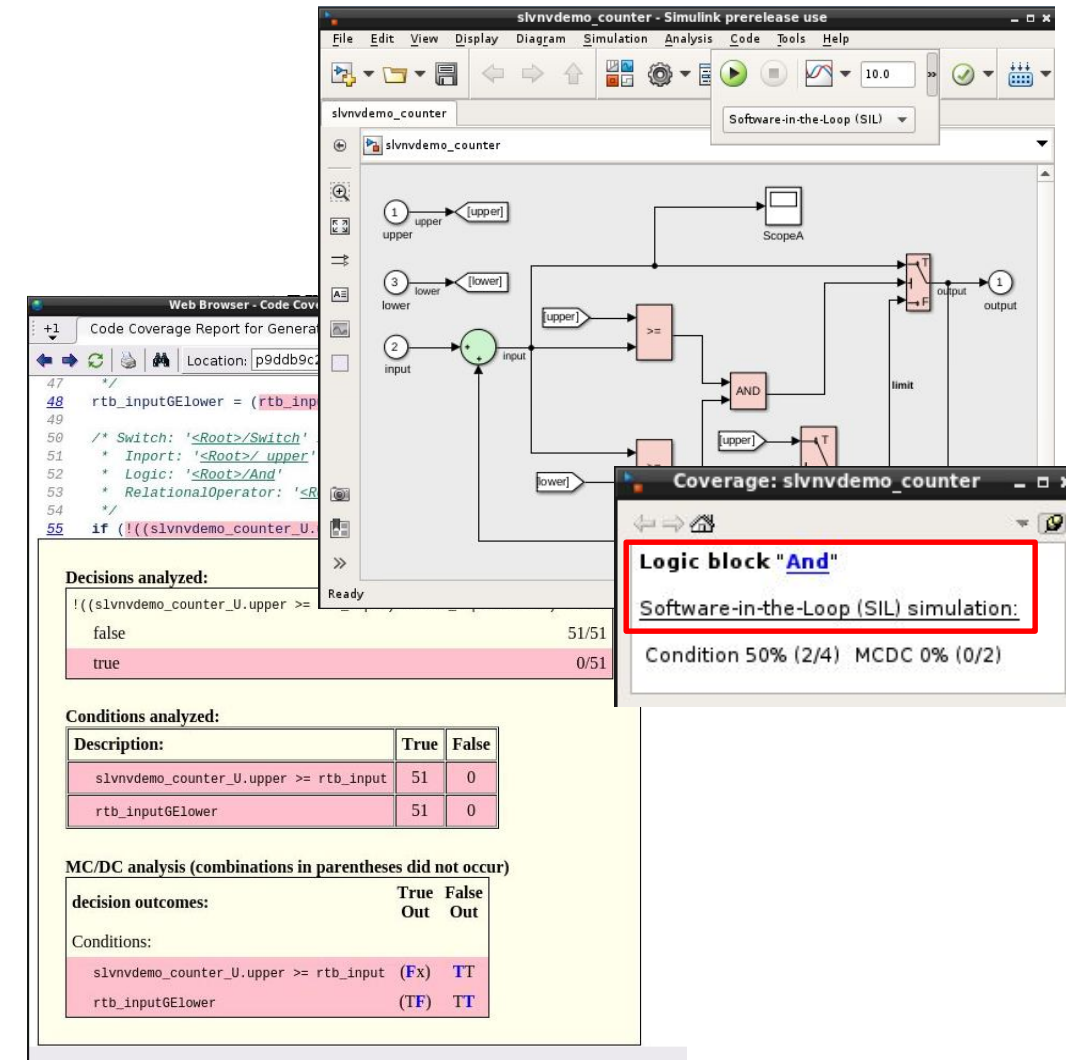


- Coverage metric
 - Measure of how much system has been tested
- Identify testing gaps to find
 - Untested design elements
 - Dead logic and unreachable states
- Identify requirement issues
 - Missing or inconsistent functional requirements
 - Discover requirement problems early
- *Product: Simulink Coverage**

Simulink Coverage

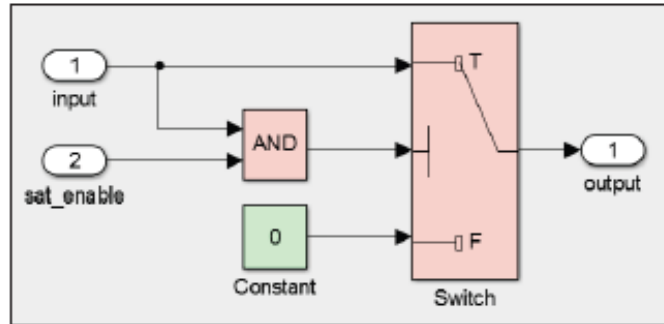
Measure test coverage in models and generated code

- Structural coverage analysis and reports from tests performed on Simulink® models (including C/C++ S-functions)
- Coverage metrics including decision, condition, MC/DC, relational boundary, and signal range
- Coverage analysis of C/C++ code generated by Embedded Coder®
- Coverage result highlighting in blocks, subsystems, and state charts
- Tool qualification support (with DO Qualification and IEC Certification Kits)



Model Elements That Receive Coverage

Simulink models

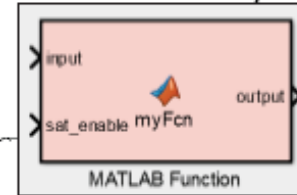


MATLAB function blocks

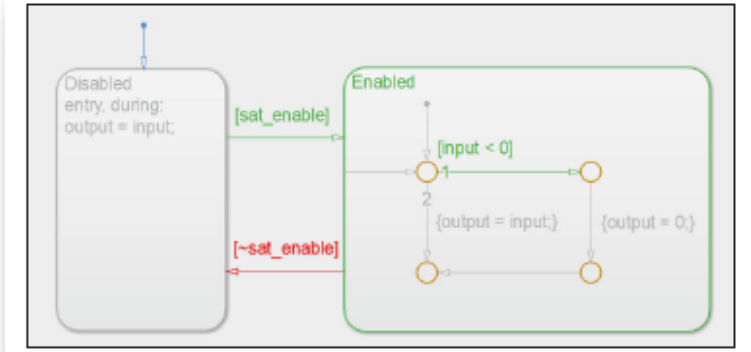
```

1 function output = myFcn(input,sat_enable)
2 %codegen
3
4 if (input<0 && sat_enable)
5     output = 0;
6 else
7     output = input;
8 end

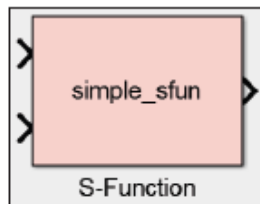
```



Stateflow charts



C/C++ code S-Functions



Decisions analyzed:

<u>!(input<0) && !sat_enable</u>	50%
false	101/101
true	0/101

Conditions analyzed:

Description:	True	False
<u>input<0</u>	50	51
<u>!sat_enable</u>	0	50

Generated code

```

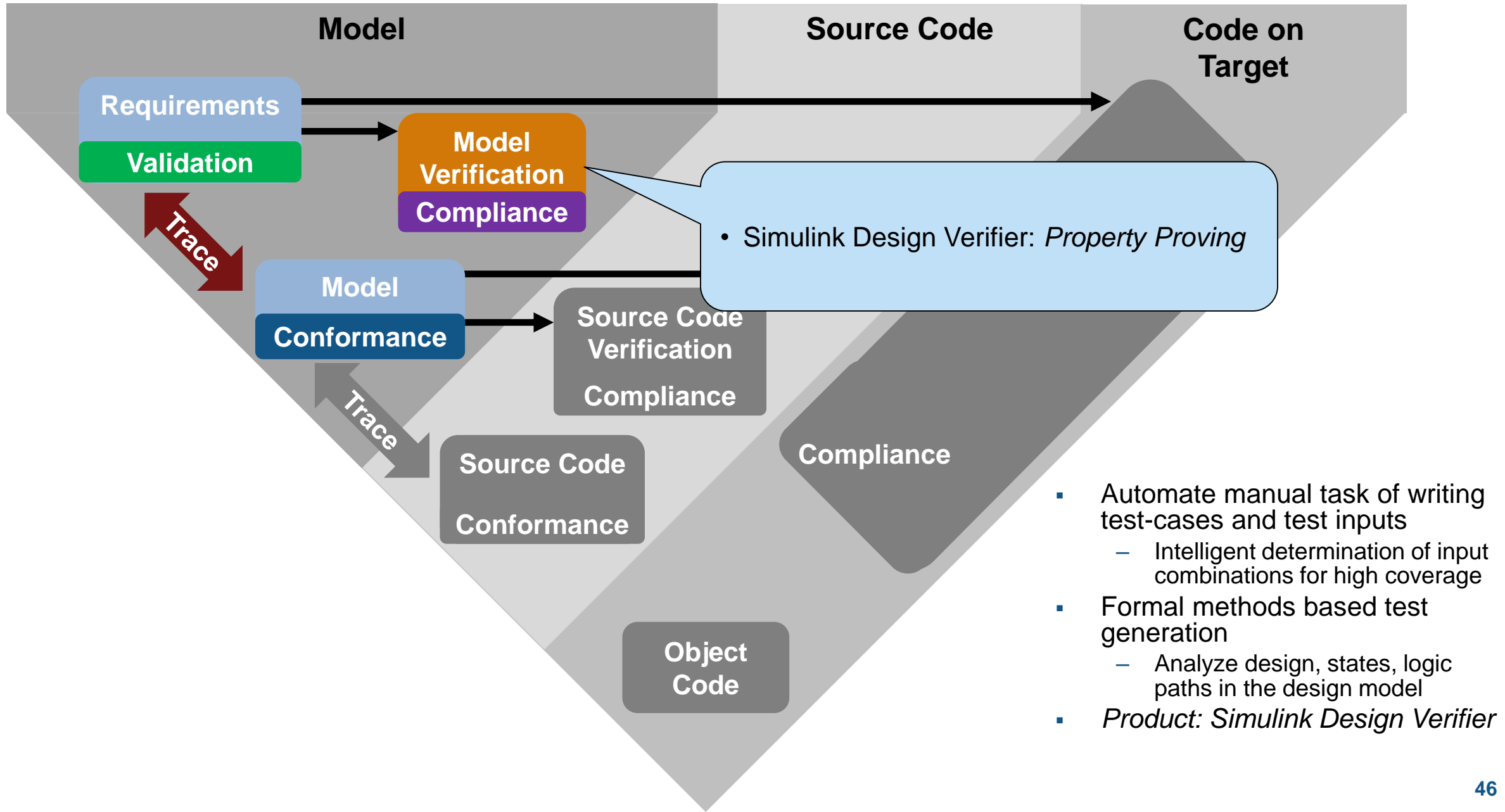
47 /*
48 rtb_inputGElower = (rtb_input >= slvnvdemo_counter_U.lower);
49
50 /* Switch: '<Root>/Switch' incorporates:
51 * Inport: '<Root>/upper'
52 * Logic: '<Root>/And'
53 * RelationalOperator: '<Root>/upper GE input'
54 */
55 if (!((slvnvdemo_counter_U.upper >= rtb_input) && rtb_inputGElower)) {

```

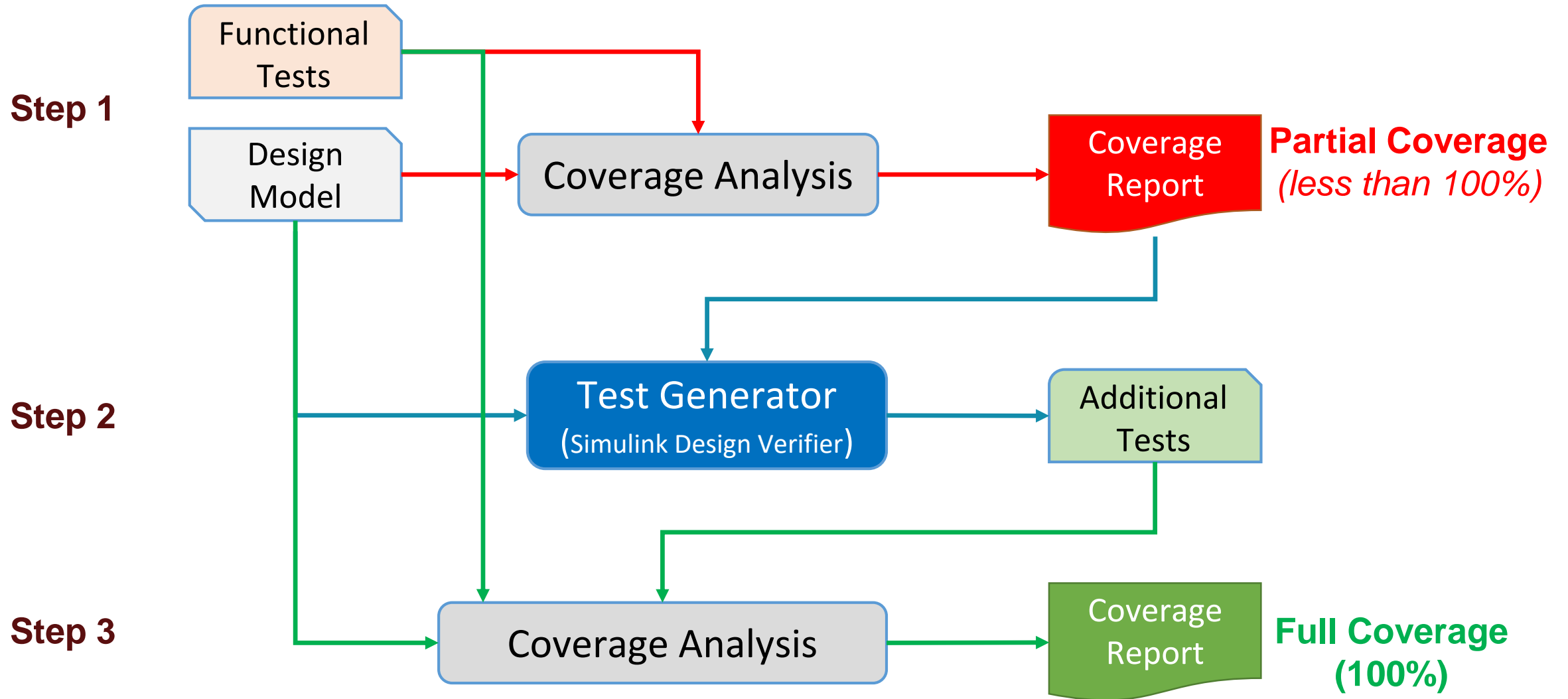
Decisions analyzed:

<u>!((slvnvdemo_counter_U.upper >= rtb_input) && rtb_inputGElower)</u>	50%
false	51/51
true	0/51

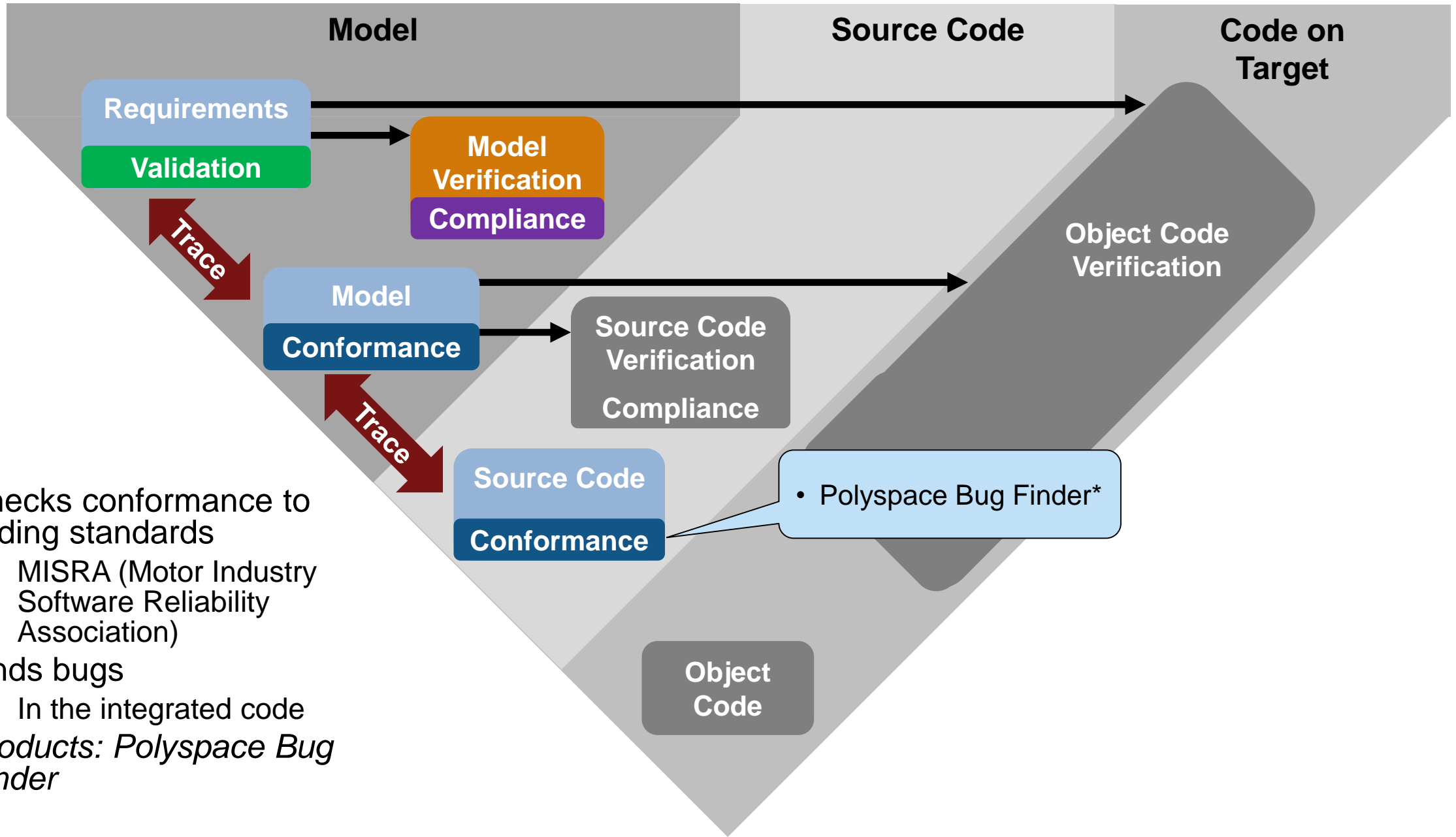
Verification and Validation Tasks and Activities



Addressing Missing Coverage

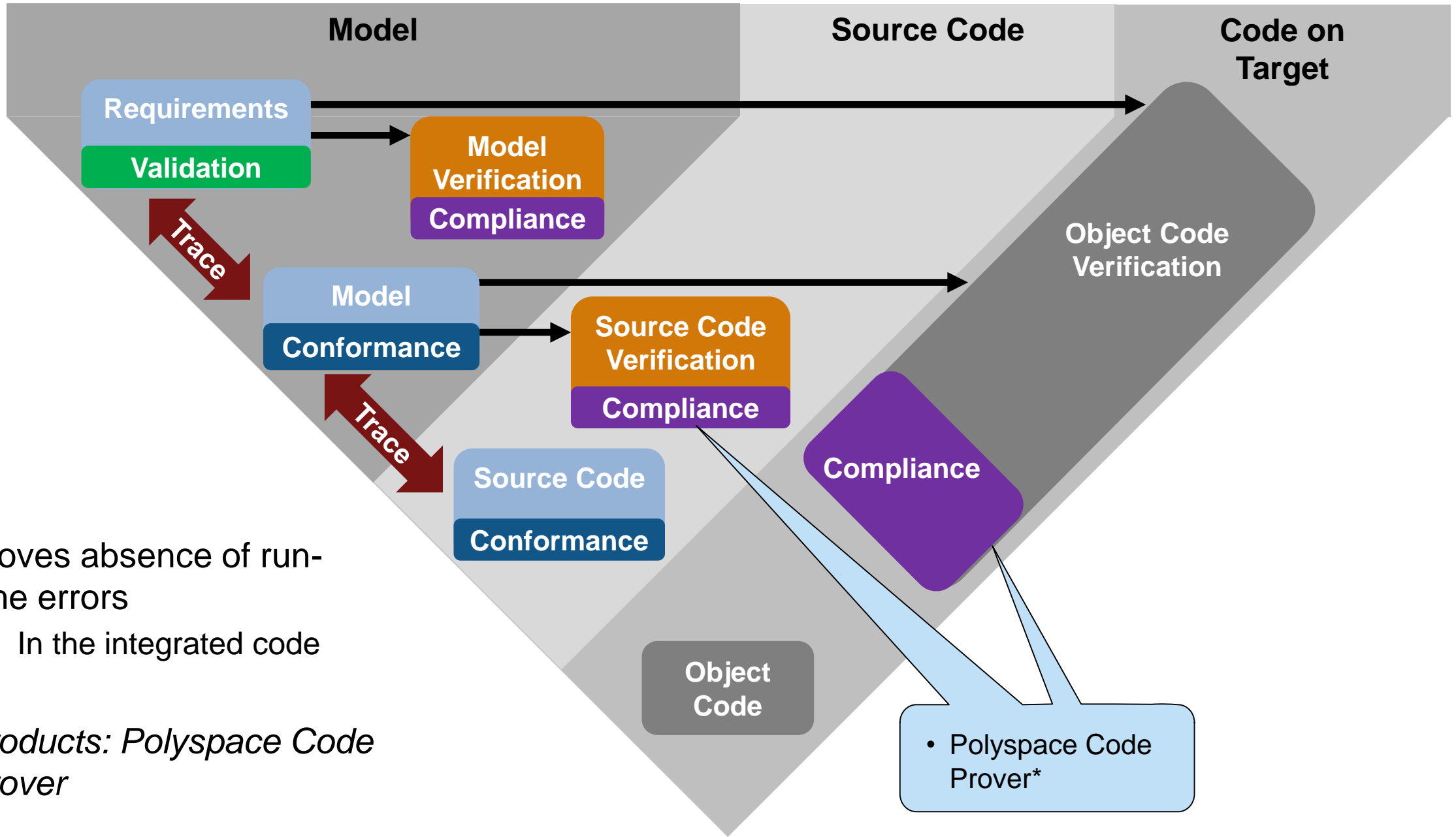


Verification and Validation Tasks and Activities



- Checks conformance to coding standards
 - MISRA (Motor Industry Software Reliability Association)
- Finds bugs
 - In the integrated code
- *Products: Polyspace Bug Finder*

Verification and Validation Tasks and Activities



- Proves absence of run-time errors
 - In the integrated code
- Products: Polyspace Code Prover

Static Code Analysis Techniques Supported by Polyspace

- Code metrics and standards
 - Comment density, cyclomatic complexity,...
 - MISRA and Cybersecurity standards
- Bug finding
 - Data and control flow of software
 - Check code for security vulnerabilities
- Code proving
 - Formal methods with abstract interpretation
 - No false negatives

The screenshot displays a C code snippet with several static code analysis findings highlighted by Polyspace. The findings are categorized by color and type:

- Green: reliable** (safe pointer access): Points to the `i++` increment in the `for` loop.
- Red: faulty** (out of bounds error): Points to the `*p = 0;` assignment, with a tooltip indicating a variable 'l' (int32) range of [0 .. 99] and an assignment of 'l' (int32) range of [1 .. 100].
- Gray: dead** (unreachable code): Points to the `*p = 5;` assignment, which is unreachable due to a preceding `if` condition.
- Orange: unproven** (may be unsafe for some conditions): Points to the `i++` increment, indicating a potential unsafe condition.
- Purple: violation** (MISRA-C/C++ or JSF++ code rules): Points to the `*p = 10;` assignment, indicating a violation of a code rule.
- Range data** (tool tip): A dashed line points to the `i` variable in the `if (i >= 0)` condition.

```
static void pointer_arithmetic (void) {
    int array[100];
    int *p = array;
    int i;

    for (i = 0; i < 100; i++) {
        *p = 0;
        p++;
    }

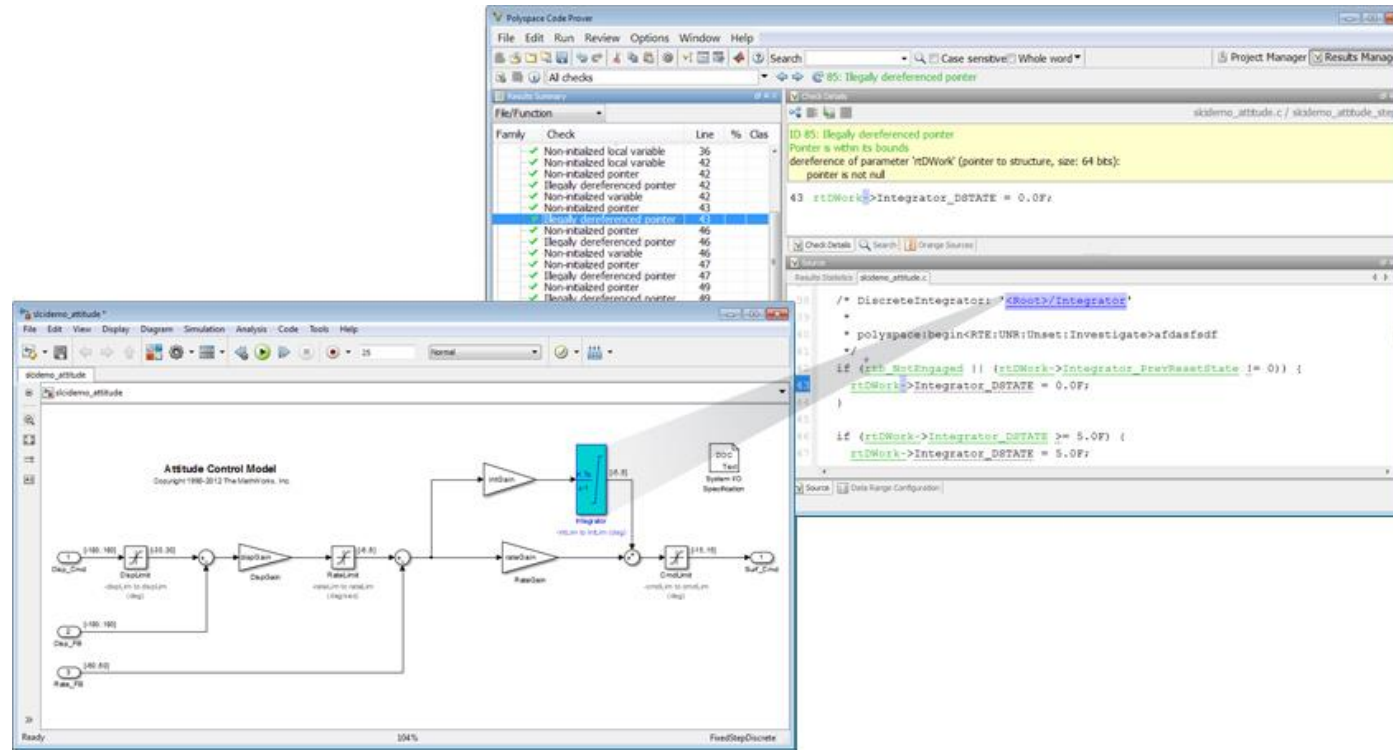
    if (get_bus_status() > 0) {
        if (get_oil_pressure() > 0) {
            *p = 5;
        } else {
            i++;
        }
    }

    i = get_bus_status();

    if (i >= 0) {
        *p = 10;
    }
}
```

Results from Polyspace Code Prover

Traceability from Code to Model



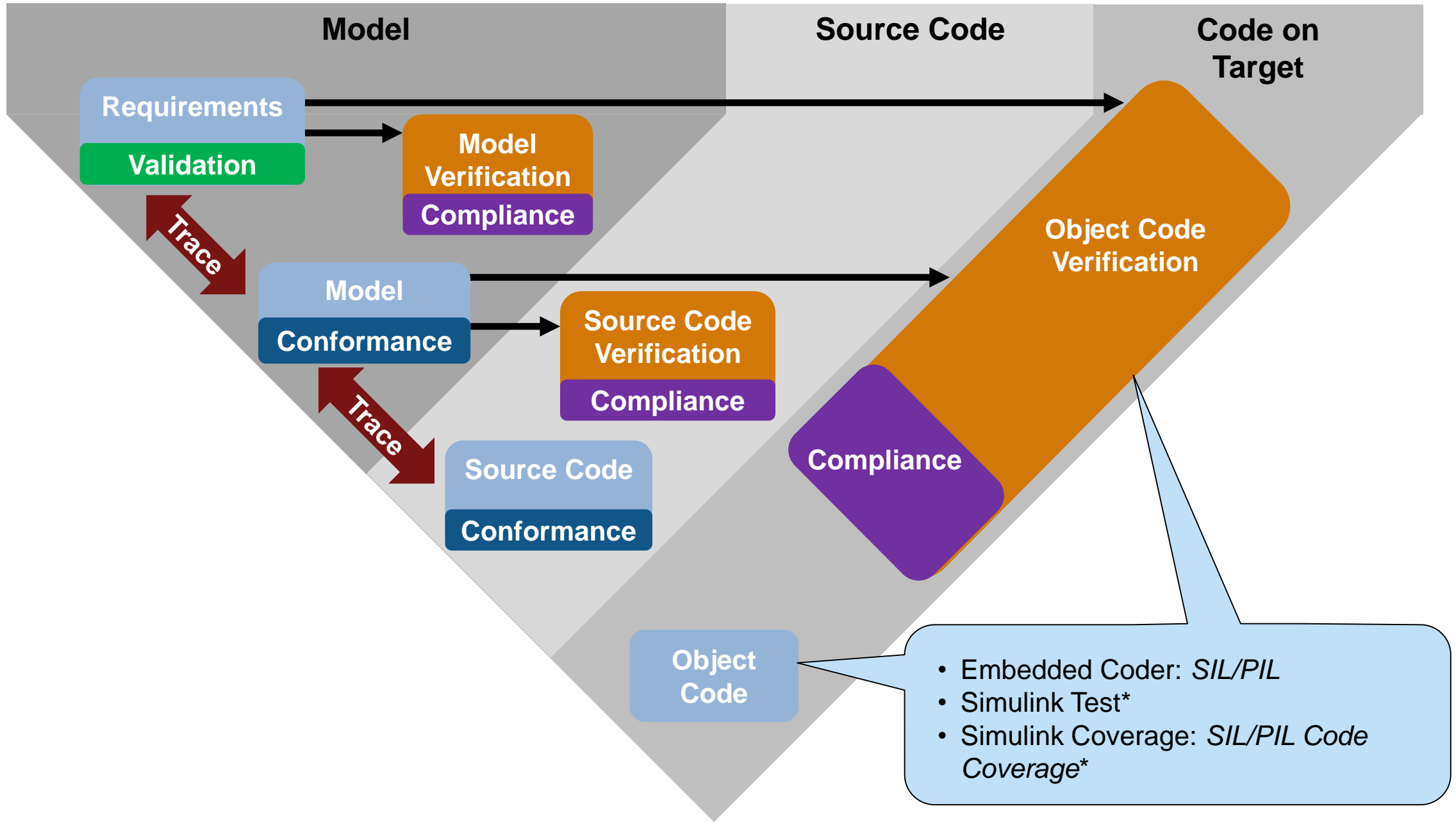
The image displays three windows illustrating the traceability from code to model:

- Polyspace Code Prover:** Shows a table of verification results for the 'File/Function' 'skidemo_attitude.c / skidemo_attitude_step()'. The table lists various checks such as 'Non-initialized local variable', 'Non-initialized variable', 'Non-initialized pointer', and 'Non-initialized port'. The results are categorized by 'Line' and '% C/C++'.
- Polyspace Bug Finder:** Displays a detailed view of a specific bug (ID 85: 'Illegally dereferenced pointer'). It provides a description of the error, the location in the code, and the specific code snippet that caused the issue.
- Polyspace Model:** Shows a block diagram of the 'Attitude Control Model'. The model includes blocks for 'Data_Snd', 'Data_Rx', 'Rate_Rx', 'Rate_Snd', 'Integrator', and 'Sum'. The model is connected to a 'Test System I/O System'.

The traceability is demonstrated by the arrows pointing from the code snippets in the Polyspace Bug Finder window to the corresponding blocks in the Polyspace Model window, showing how the code is mapped to the model components.

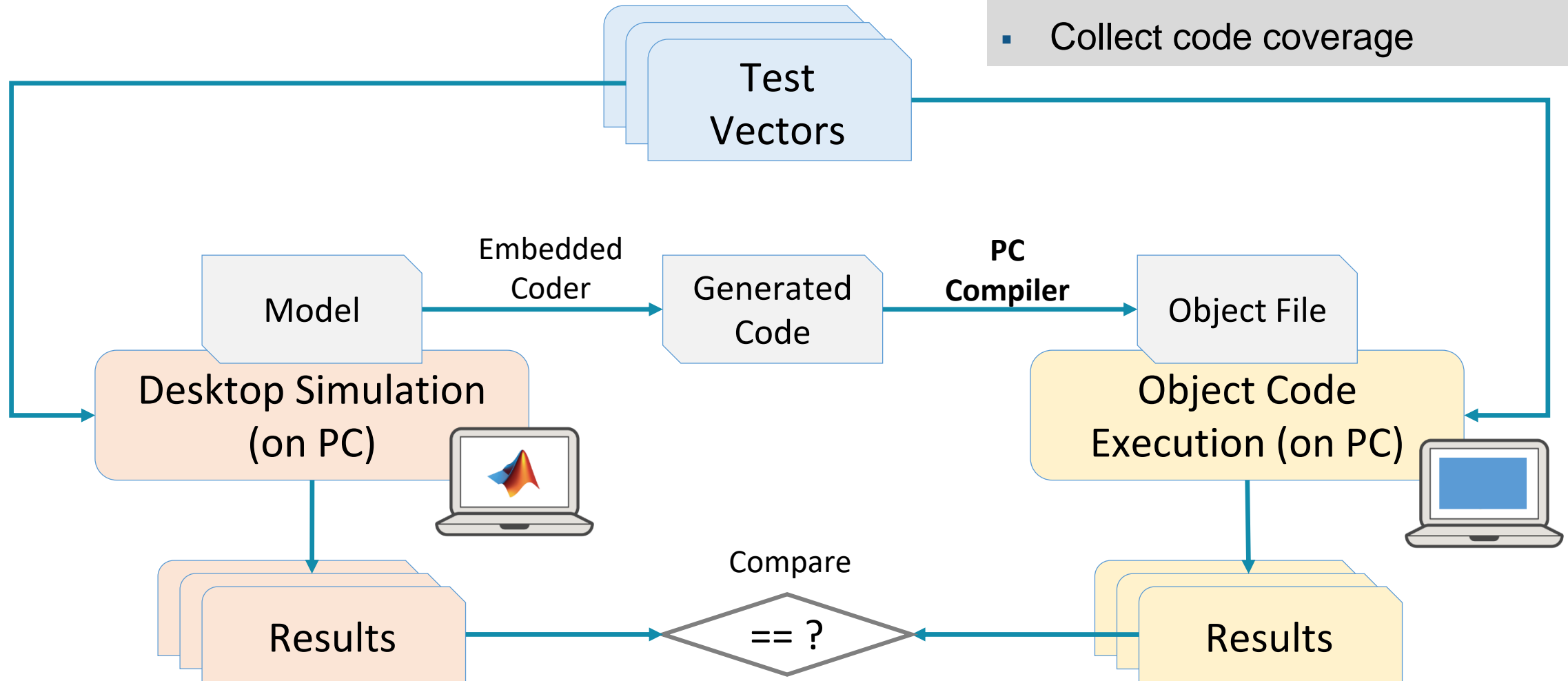
Polyspace Bug Finder and Polyspace Code Prover verification results, including MISRA analysis can be traced from code to model

Verification and Validation Tasks and Activities



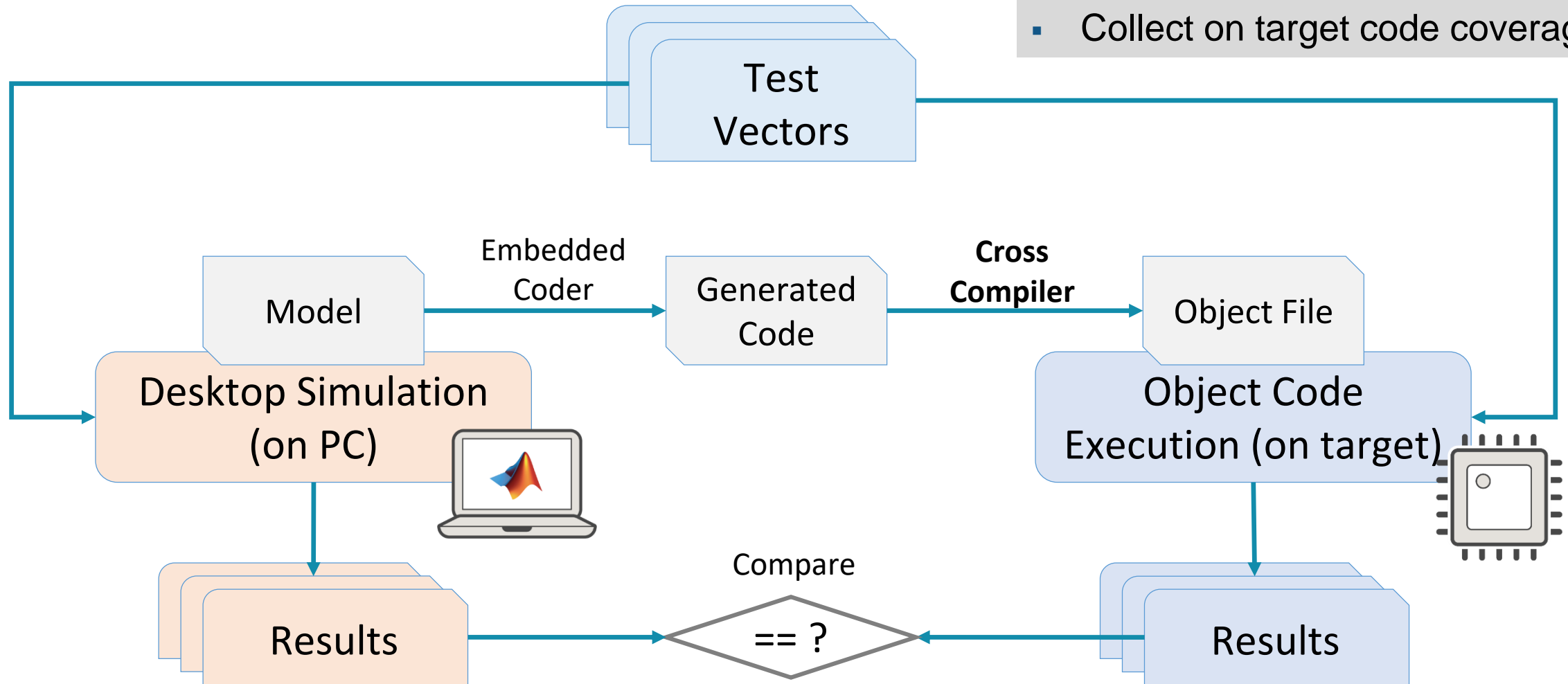
Software In the Loop (SIL) Testing

- Show equivalence, model to code
- Assess code execution time
- Collect code coverage



Processor In the Loop (PIL) Testing

- Verify numerical equivalence
- Assess target execution time
- Collect on target code coverage



MathWorks V&V Solution Summary

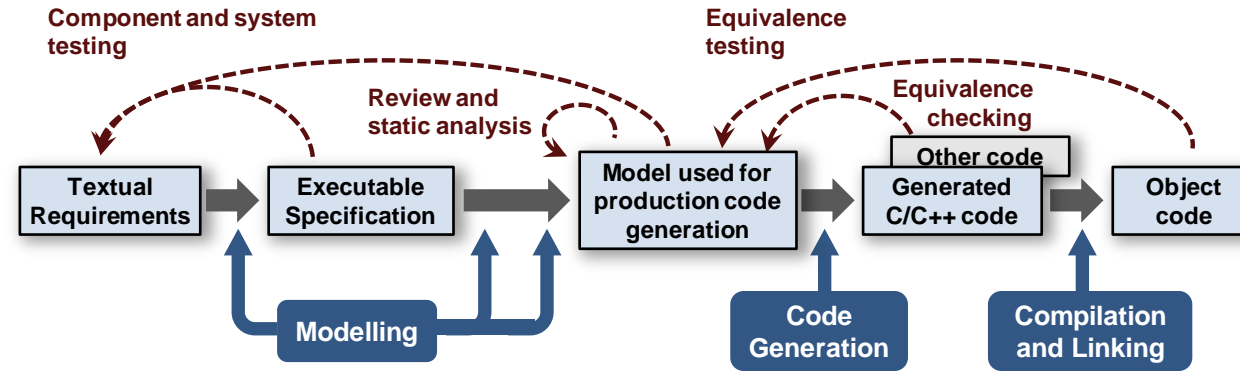
Requirements	Author, manage, and trace requirements
Standards Compliance	Verify compliance with standards and guidelines
Testing	Develop, manage, execute simulation-based tests
Formal Verification	Prove design meets requirements, prove robustness
Coverage Analysis	Measure model and generated code coverage
Static Code Analysis	Check bugs, MISRA compliance, prove code
SIL, PIL	Perform back-to-back testing

MathWorks V&V Product Capabilities

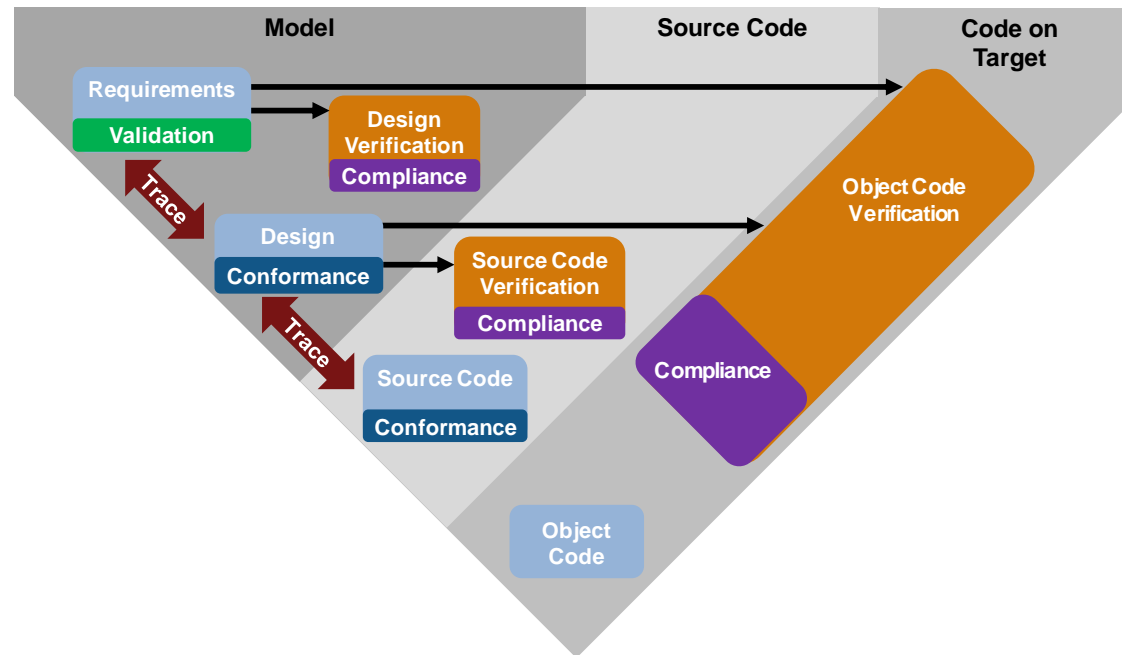
Requirements	Simulink Requirements* (<i>New in R2017b</i>)
Standards Compliance	Simulink Check* (<i>New in R2017b</i>)
Testing	Simulink Test
Formal Verification	Simulink Design Verifier
Coverage Analysis	Simulink Coverage* (<i>New in R2017b</i>)
Static Code Analysis	Polyspace Bug Finder, Polyspace Code Prover
SIL, PIL	Simulink Test

Workflows for Certification Standards

IEC 61508
ISO 26262
IEC 62405
EN 50128



DO-178C
DO-331
DO-333



Bell Helicopter Develops World's First Commercial Fly-by-Wire Helicopter

Challenge

Develop flight software for the first commercial fly-by-wire helicopter and certify it to DO-178B Level A

Solution

Use Model-Based Design to model and simulate the control laws, trace requirements to the model, and generate and verify 16,000 lines of code

Results

- Integration time cut by 90%
- Development iterations reduced from weeks to hours
- Confidence in code quality maintained
- Simulink Code Inspector Qualified by FAA for DO-178B Level A



The Bell 525 Ships 1 and 2 over the Palo Duro Canyon.

“With Model-Based Design we had a successful first flight; there were no issues from a control or integration standpoint. Generating the control law code from our Simulink model with Embedded Coder eliminated the slowdowns caused by manual code generation and freed the team to work on meeting the broader program goals.”

- Mike Bothwell, Bell Helicopter

BAE Systems Delivers DO-178B Level A Flight Software on Schedule with Model-Based Design

Challenge

Develop flight-critical software for a midsized business jet in compliance with DO-178B Level A standards

Solution

Use Model-Based Design to model the software and systems, run simulations with customer-provided test vectors, trace requirements to model elements, and generate 200,000 lines of certified code

Results

- Development efficiency doubled
- Certification schedule maintained
- Communication between teams facilitated



Primary flight control computers from BAE Systems.

“When we generated code from our Simulink models with Embedded Coder, the team we handed it off to knew it was gold—that it was debugged and fully met the requirements—because we had run it through the Simulink test vectors supplied by our customer. That was a huge advantage on this program.”
- Maria Radecki, BAE Systems

ESA and Airbus Create Upper-Stage Attitude Control Development Framework Using Model-Based Design

Challenge

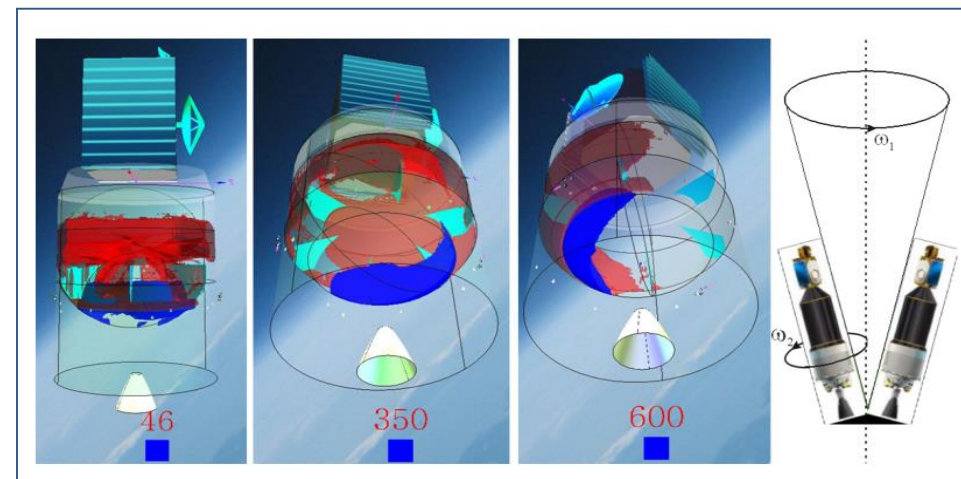
Speed the development of software for controlling complex launcher upper stage missions including the attitude of satellite payloads after they separate from ESA launch vehicles

Solution

Use Model-Based Design to develop controller models and multidomain physical models, run closed-loop simulations, and generate code for PIL testing

Results

- Design iterations reduced from one week to one day
- Failure modes modeled and eliminated
- Comprehensive design framework established



Propellant motion in spinning upper stages at 46, 350, and 600 seconds. Distribution after 350 seconds becomes uneven

“Model-Based Design multiplies the range of capabilities that I have as an engineer. As an individual control engineer I can do what previously took a handful of engineers, because I can create and simulate my own multidomain models. I don’t have a wall around me anymore; I am able to better communicate and contribute across disciplines.”

- Samir Bennani, ESA

Contact Us

508-647-7000

Monday - Friday

Customer Support 08:30-17:30 ET

Technical Support 08:30-20:00 ET



