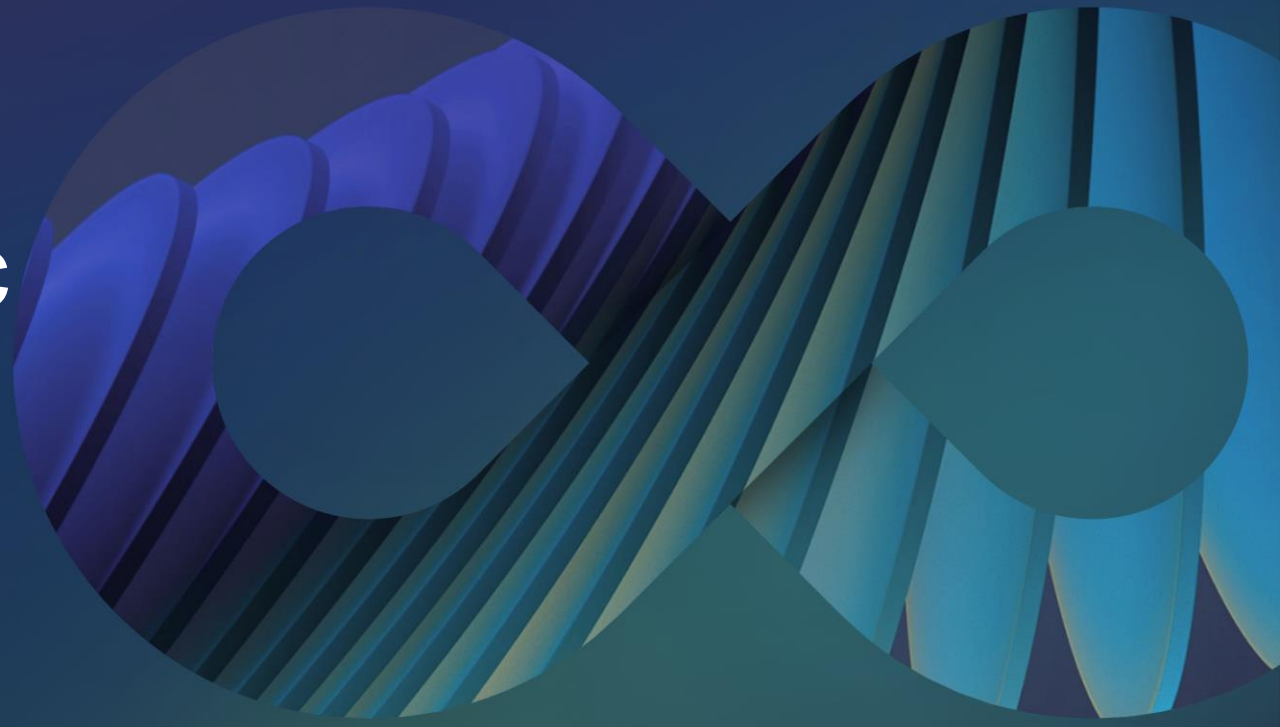
Model-Based Cybertronic Systems Engineering



Challenges, Methodology and Solutions

Ahmed Hamza

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The Cybertronics Challenge

Cybertronics

The engineering discipline of hw/sw functional co-architecture to realize new s/w defined, semiconductor enabled systems.

It requires a new, advanced form of model-based systems engineering that drives cybertronics design automation; MBCSE

Cybertronics Design Automation

MBCSE-driven EDA = Architecture Analysis + Digital Threading + conventional EDA = Cybertronics Design Automation

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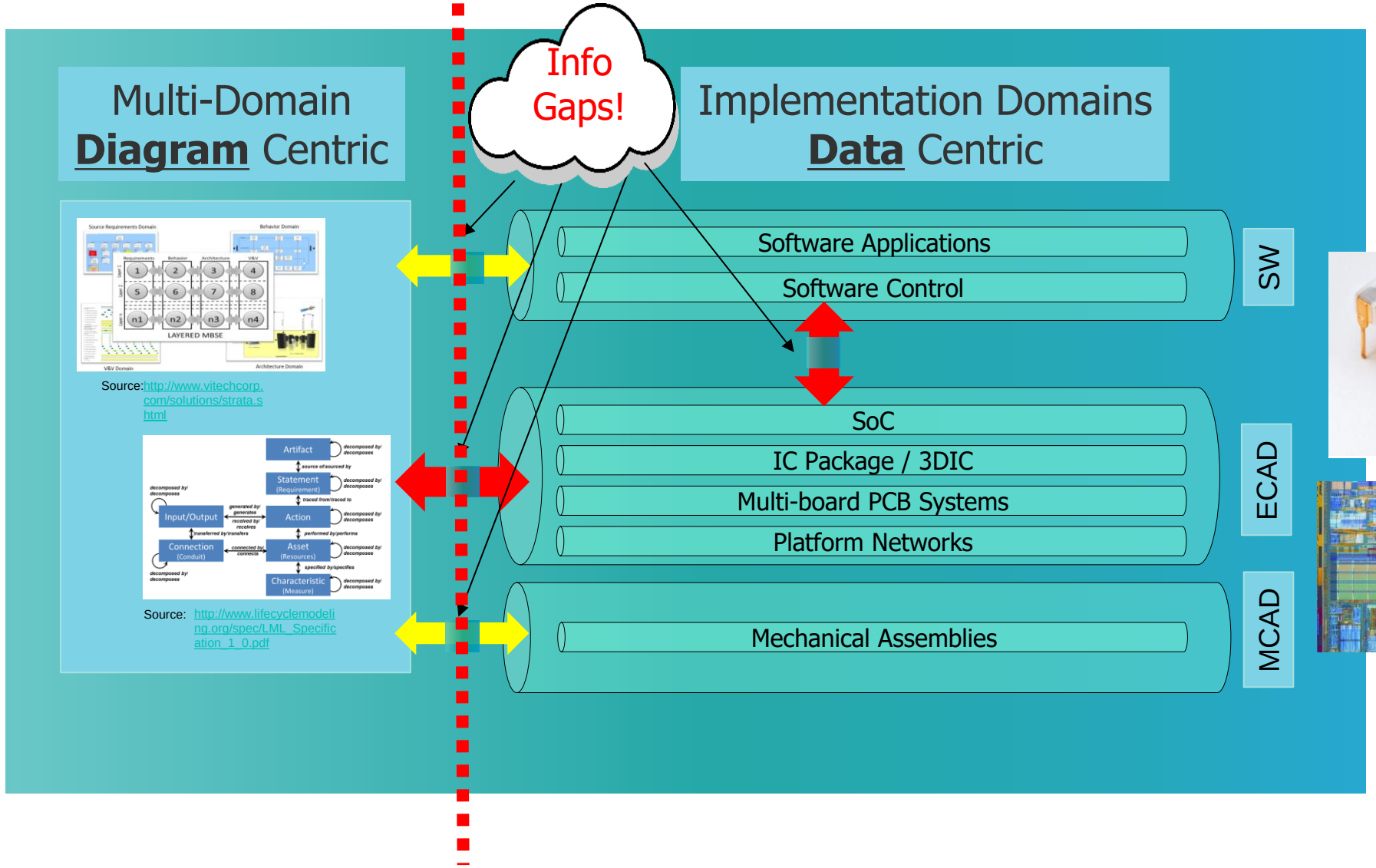
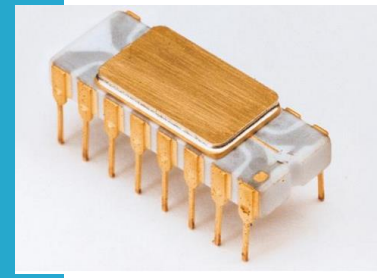
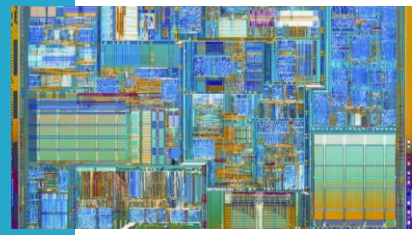
Cybertronics Engineering Status: Systems Engineering is not Model-Based enough







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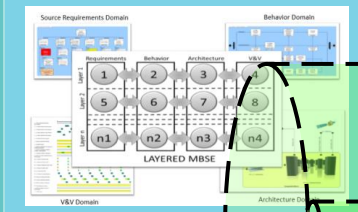
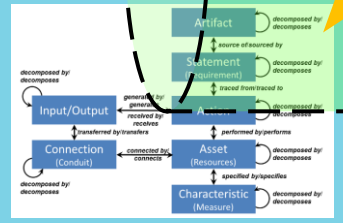
Future Status: Cybertronics Systems Engineering Driven EDA

Multi-Domain
Diagram Centric



Source:http://www.vitechcorp.com/solutions/strata.shtml



Source: http://www.lifecyclemodeling.org/spec/LML_Specification_1_0.pdf

Implementation Domains
Data Centric

- Software Applications
- Software Control
- Hardware/Firmware/Software
- ~~SoC~~
- IC Package / 3DIC
- Multi-board PCB Systems
- Platform Networks
- Mechanical Assemblies

SW
CT
ECAD
MCAD

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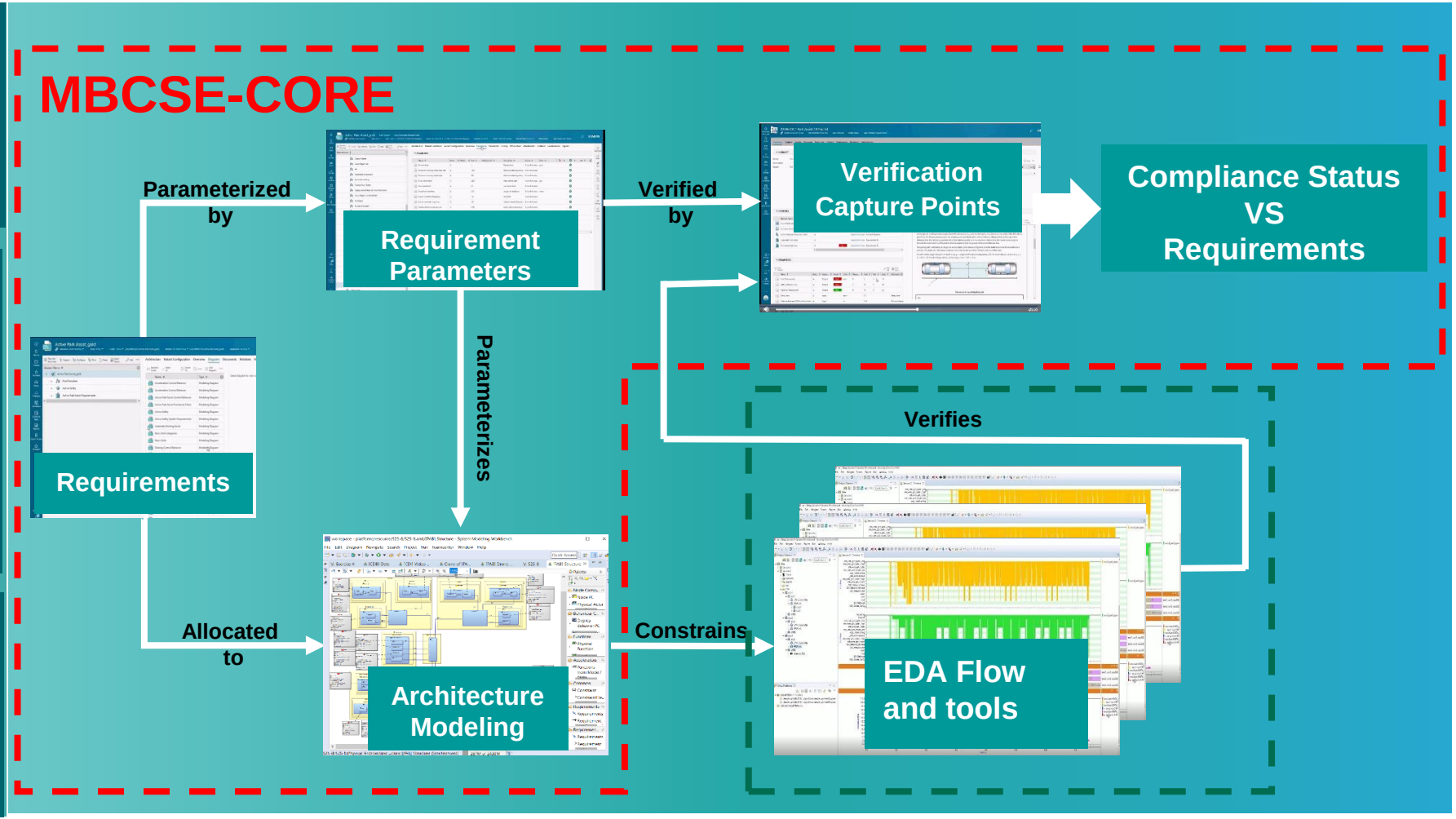
MBCSE-CORE Framework

The MBCSE-CORE enables requirements engineering, system modeling and verification management

SoSS architecture modeling requires explicit abstractions for Functional, Logical and Physical Layers, as well as black box / white box transitions between sub-systems

Domain specific tools will interact with the MBCSE-CORE on a fit-for-purpose basis, as optional extensions



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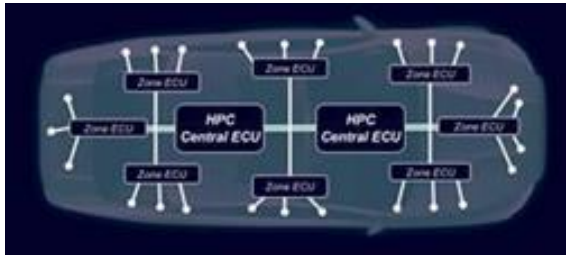
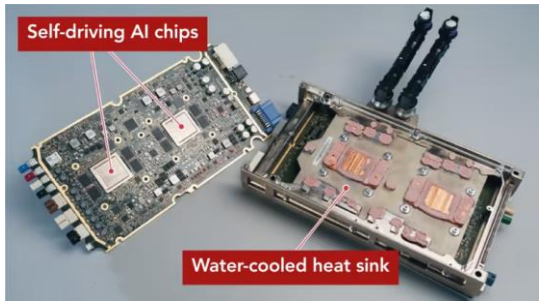
System Functional Allocation with Verifiable Requirements is Non-Existent



Platform Network

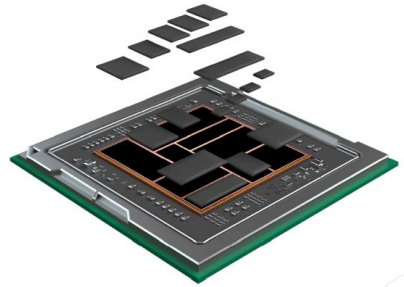
Refined Requirements
Decomposed Functions
Analyzed Architectures
Design Verifications
Technical Baselines



Compute Enclosure

Requirements
Functions
Notional Architectures

Aggravated by weakness of standards and integrations



3DIC / SoC

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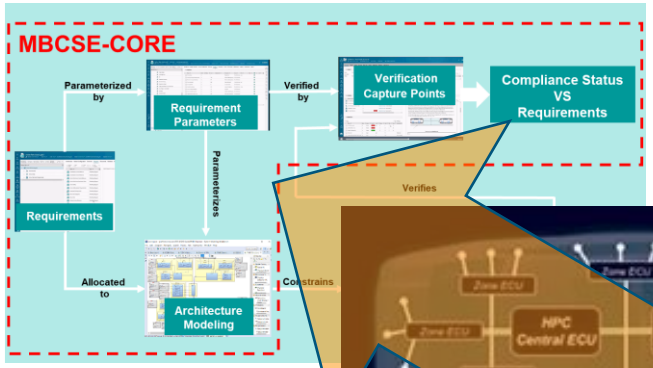
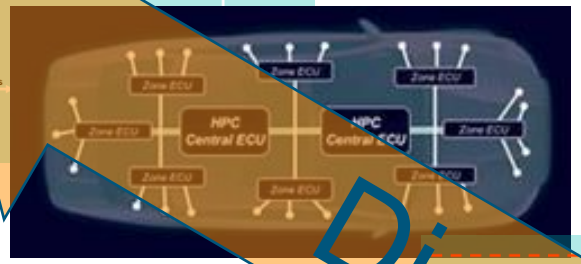
MBCSE Enables Threading of Functional Allocation and Verifiable Requirements for Systems of Cybertronic Sub-Systems

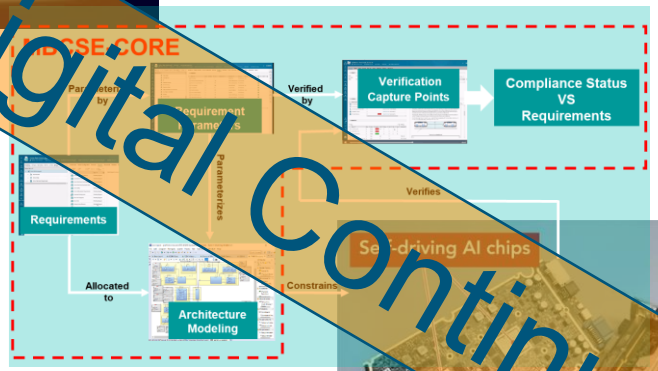




Platform Network

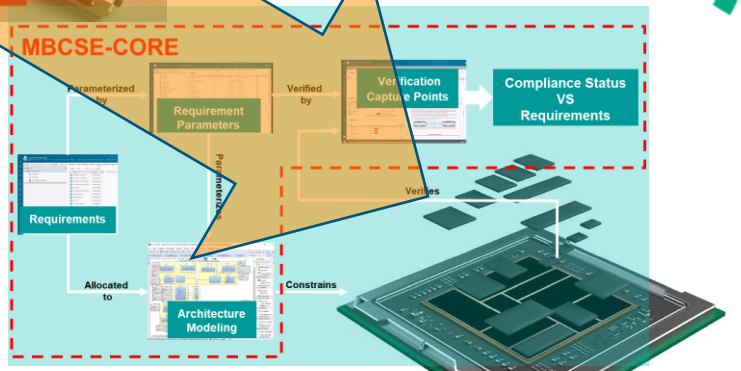
Digital Continuity

Threaded Verification



Compute Enclosure

Threaded Requirements



Reference SoCSS Model

3DIC / SoC

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Cybertronic Definition and Focus

Cybertronics

Can be described as the collective methods, Automation technologies, and processes to help study, analyze, and design software-defined electronic systems

- System of system Knowledge capture
- Top-down knowledge traceability
- Reusability
- Parameter/requirement traceability
- Early verification
- Cross-enterprise Collaboration

Why EDA need MBCSE

MBCSE Hardware and Software performance analysis

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Why

System Complexity

Domains, control, power, etc.

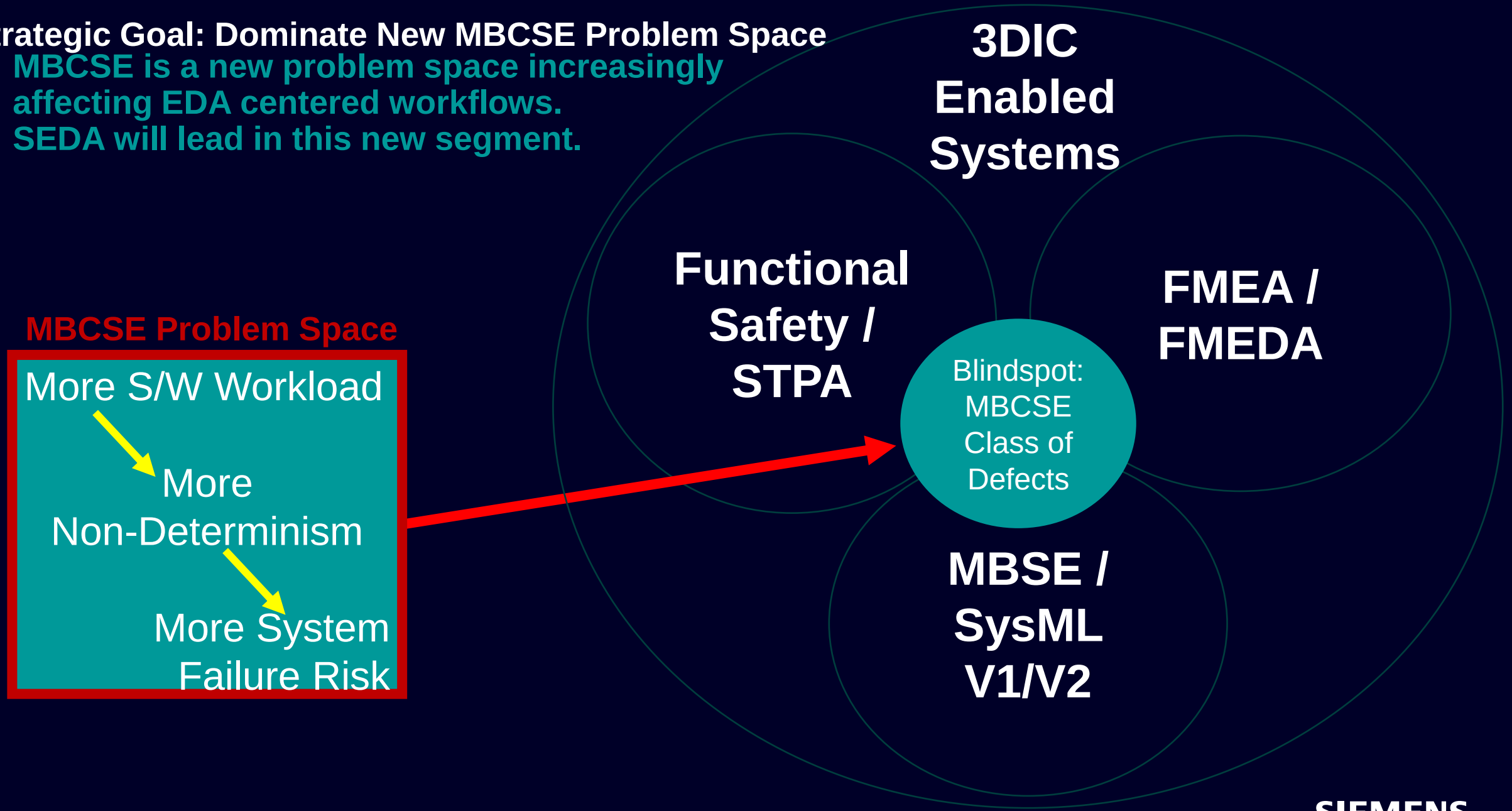
End Application Complexity

Algorithm performance, HW/SW, etc.

- Explosion in **time-sensitive**, heavy compute software loads running on customized and optimized hardware
- Complexity increases and cycle time decreases
- Silo System engineering practice, lose sight of the big picture
- Digitization of paper – data within these documents is still static and disconnected

Strategic Goal: Dominate New MBCSE Problem Space

- MBCSE is a new problem space increasingly affecting EDA centered workflows.
- SEDA will lead in this new segment.



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The Current Status of System Engineering

SysML v1 – Cameo **vs SysML v2**

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The Industry is Failing to Share SE Information Reported at GPDIS Oct'20

GLOBAL PRODUCT DATA INTEROPERABILITY SUMMIT

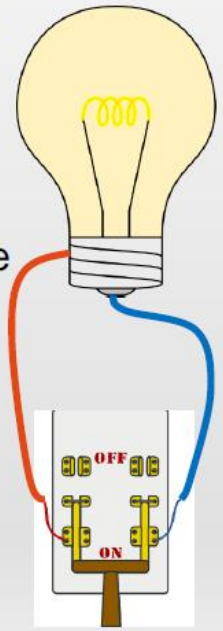
A&D PLM Action Group- MBSE Project Data Exchange Trials

Phase 1 Results

The Light Switch Example

OEM Role:
Create a simple model
Allocate requirements
Share with Supplier

Supplier Role:
Open model
Make a simple change
Resend to OEM



MBSE Data Exchange Trials		All participants prepared OEM SCD & Tecnhical Data Package; All models and Trial results data uploaded into AirCollab project folders				Red= Faliure Grey= Partial Success Green= Success	Red= Faliure Grey= Partial Success Green= Success
Round 1	**OEM Role**	**OEM Modeling Tools Used**	**Data Export Standards Used**	**Supplier Role**	**Supplier Tools Used**	**Trial Outcome (System Model)**	**Trial Outcome (Requirements)**
	Boeing	MagicDraw v18.1	UML 2.5 XMI	GE	IBM Rhapsody v8.2.1	Failure	Failure
	Boeing			Rolls-Royce	PTC Integrity v8.3.18 & Enterprise Architect, DOORS v9.5	Failure	Partial Success
	Boeing	DOORS v9.6	ReqIF v1.1	Airbus	IBM Rhapsody v8.1.4	Failure	Failure
Round 2	**OEM Role**	**OEM Modeling Tools Used**	**Data Export Standards Used**	**Supplier Role**	**Supplier Tools Used**	**Trial Outcome (System Model)**	**Trial Outcome (Requirements)**
	Airbus	IBM Rhapsody v8.1.4 (Reqs Included in SysML model)	XMI	Rolls-Royce	PTC Integrity v8.3.18 DOORS v9.5	Failure	Failure
	Airbus			GE	IBM Rhapsody v8.2.1	Failure	Failure
	Airbus			Boeing	Rhapsody 8.1.5	Failure	Partial Success
	Rolls-Royce	PTC Integrity Modeler v8.3.18	XMI	Boeing	Rhapsody 8.1.5	Failure	Failure
	Rolls-Royce			GE	IBM Rhapsody v8.2.1 DOORS NG	Failure	Partial Success
	Rolls-Royce	DOORS v9.5	ReqIF v1.0	Rolls-Royce	PTC Integrity Modeler v8.3.18	Failure	Partial Success
	GE	IBM Rhapsody v8.2.1	UML 2.3 XMI	Boeing	Rhapsody 8.1.5	Failure	Failure
	GE	DOORS NG	ReqIF v1.2	Rolls-Royce	PTC Integrity v8.3.18 DOORS v9.5	Failure	Failure

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SysML is not living up to the hype

Four critiques of SysML:

1. The learning curve is too steep
2. The mechanics are cumbersome
3. The barriers to organizational adoption are high
4. It is rarely used past the concept stage

(26) Post | LinkedIn

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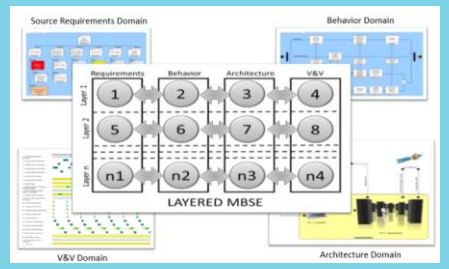
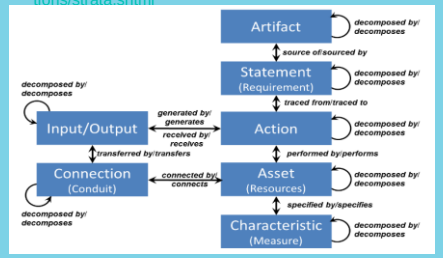
Current Status: Systems Engineering is not yet Model-Based enough

1

Multi-Domain
Diagram Centric



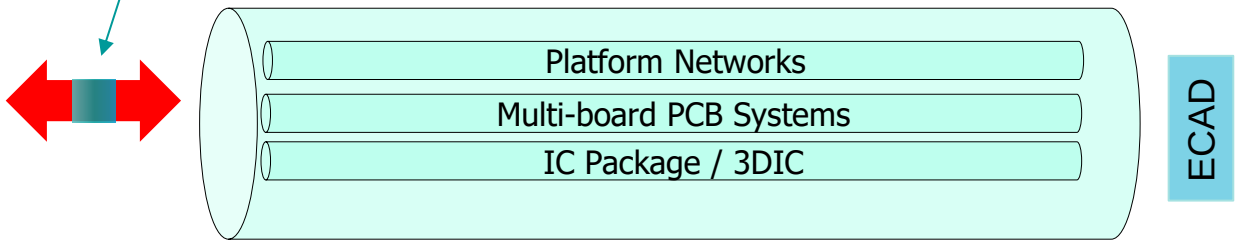
Source: http://www.vitechcorp.com/solutions/strata.shtml



Source: http://www.lifecyclemodeling.org/spec/LML_Specification_1_0.pdf

Integration Gaps!

Implementation Domains
Data Centric



Non-Deterministic database

Deterministic database

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Lack of Standard profile

2

SysML V1

All profiles and libraries bundled with CAMEO products are considered standard/system resources, non-modifiable, and essential for the proper performance of the tool.

We highly recommend not to modify our provided standard profiles and libraries as it could cause problems with version updates, plugins, core malfunctions, and model corruptions.

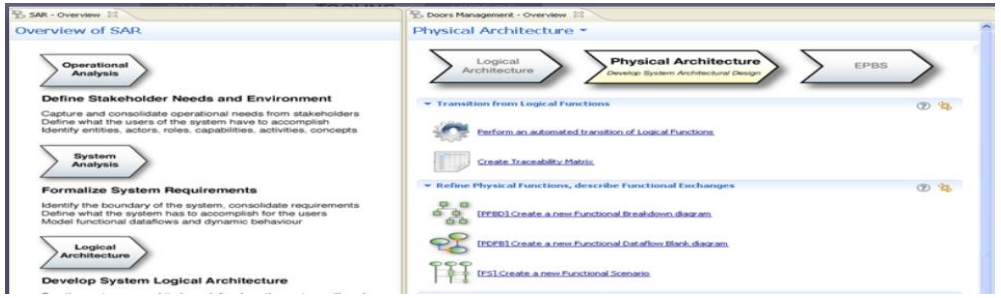
Intentional or unintentional attempt to modify profiles when:

- Opening profiles as projects.
- Using profiles in the read-write mode.
- Importing profiles into a project.
- Merging projects, and several other occasions.

AE SysML v2

Agree on a standard notation: In a team environment, it is important that others can understand your diagrams without much explanation. Choosing a standard notation enables others to quickly comprehend your diagrams without ambiguity.

The activity browser provides methodological access to all key activities of AE. It is the main entry point to a model and is both meant for beginners and power users.



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Lack of Methodology

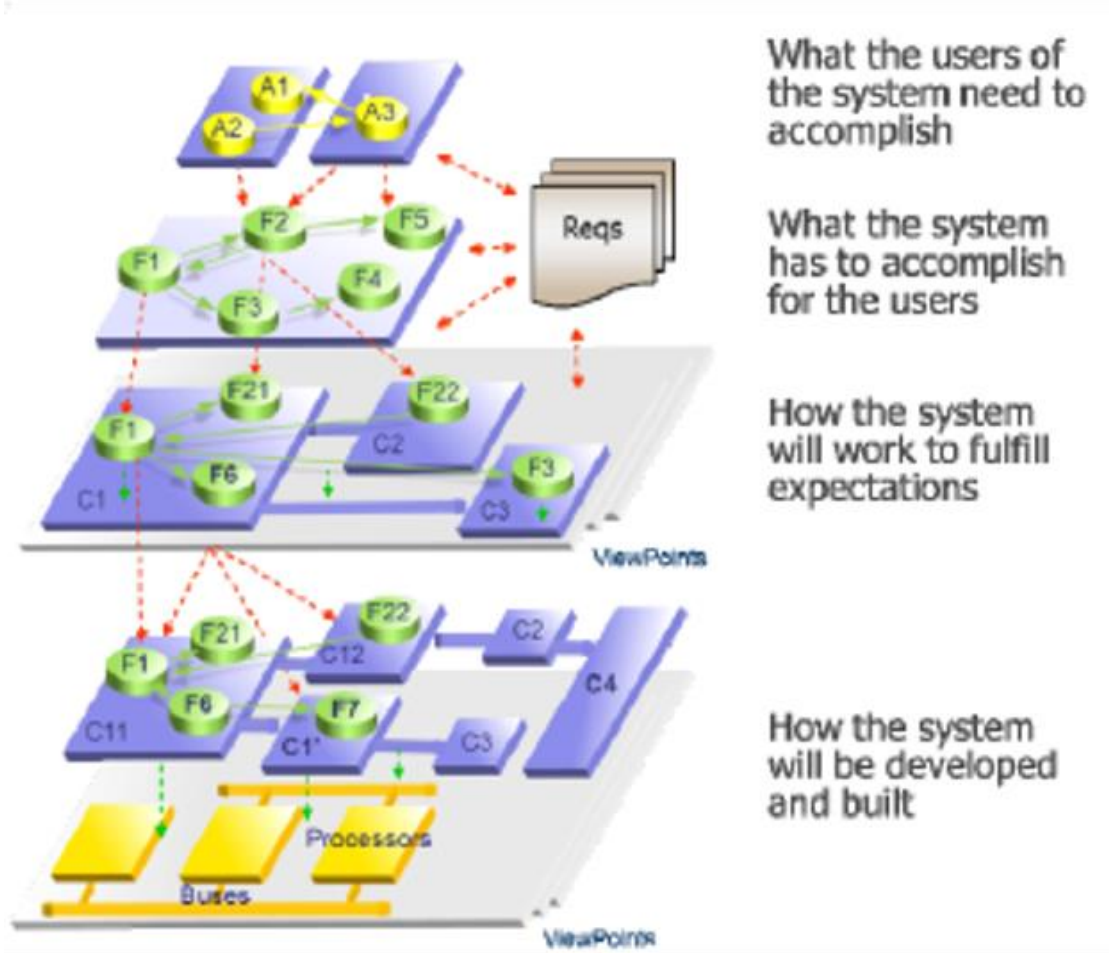
3

SysML V1

AE SysML v2

Arcadia is a tooled method devoted to systems and architecture engineering, supported by the Architecture Explorer modeling tool.

Methodological Guidance



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Use Abstraction and System to Sub-system Decomposition

4

SysML V1

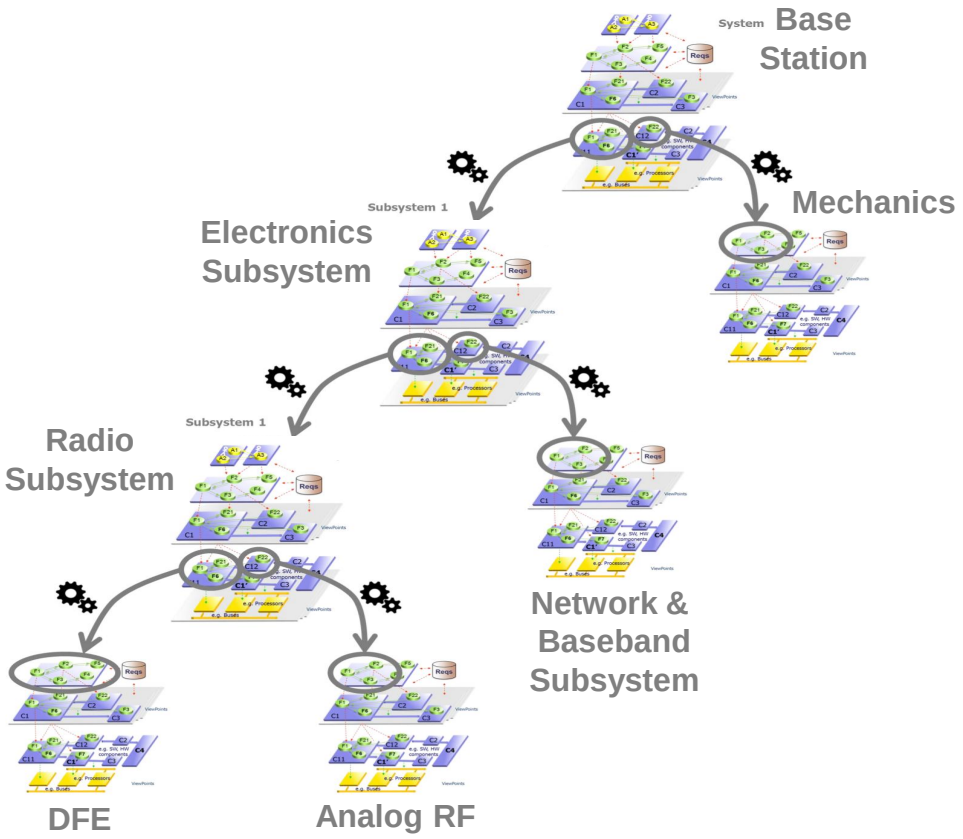
AE SysML v2

One of the most effective ways to manage system design complexity is to use abstraction and decomposition.

Abstraction is the process of hiding the details of a system and exposing only the essential characteristics and functionality.

Decomposition is the process of breaking down a system into smaller and simpler components that can be designed, implemented, tested, and maintained independently.

By using abstraction and decomposition, you can reduce the complexity of the system, increase the modularity and reusability of the components, and isolate the impact of changes.



Source: https://eclipse.dev/capella/arcadia.html

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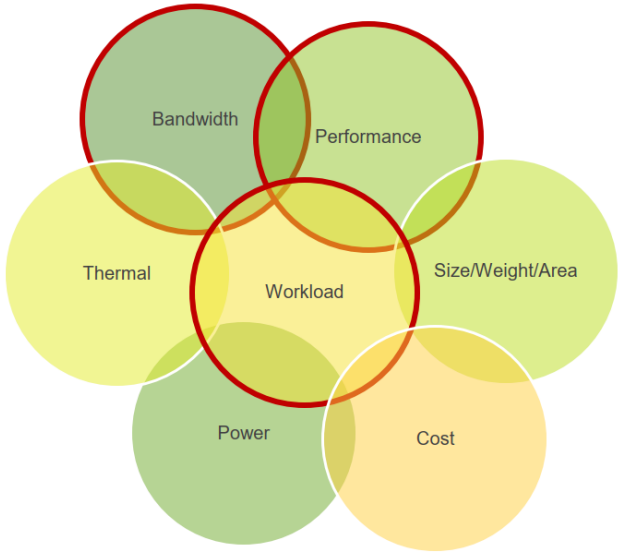
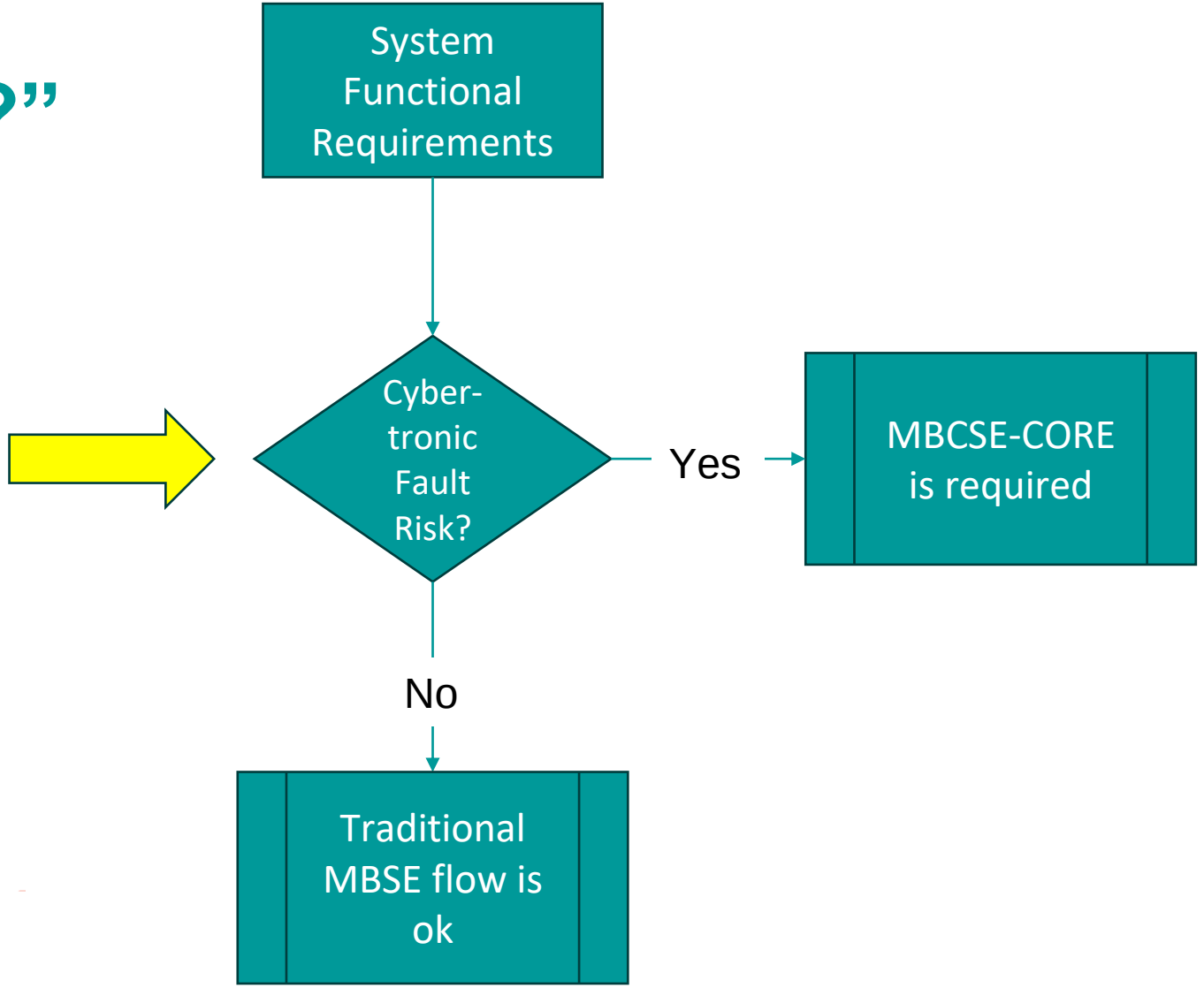
Customer Facing: “How do you allocate functionality between hardware and software?”

Does the functional workload pose a time critical risk?



Example Trade Space



System Modeling Tools Scale Value
Change from a Burden work to a Value work

+++ The tool will tell you something you don't know (emergent behavior) *

- Example language: Verilog AMS, VHDL AMS

++ The tool will analyze a huge amount of data, with all the corner cases

- Example: SystemC, network process-based simulation

+ The tool will confirm what you Believe/know by ensuring nothing has been overlooked

- Example: Simulink

0 Rehearses what you know; it's almost a waste of effort If a tool requires complete and detailed input.

That the input is just the output in a different format. "It's a pretty printer."

Most of the system design tools SysML v1

- The tool re-enforces incorrect or Incomplete thinking

- - The tool instills incorrect or incomplete thinking

* Emergent behavior is **behavior of a system that does not depend on its individual parts, but on their relationships to one another**. Thus, emergent behavior cannot be predicted by examination of a system's individual parts.

Architect Explorer

MBCSE Hardware and Software performance analysis

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Architect Explorer

- Architect Explorer is a design environment that supports the system requirements, design, analysis, verification, and validation associated with developing complex systems.
- Architect Explorer enables Digital transformation of Systems Engineering from a Document-centric engineering to Digital model-based systems Engineering.
- A digital Model environment will create a Common Standard to capture, analysis, validate, and document the system
- System Thinking is a way to examine the design sub-system part of a larger system and product life cycle

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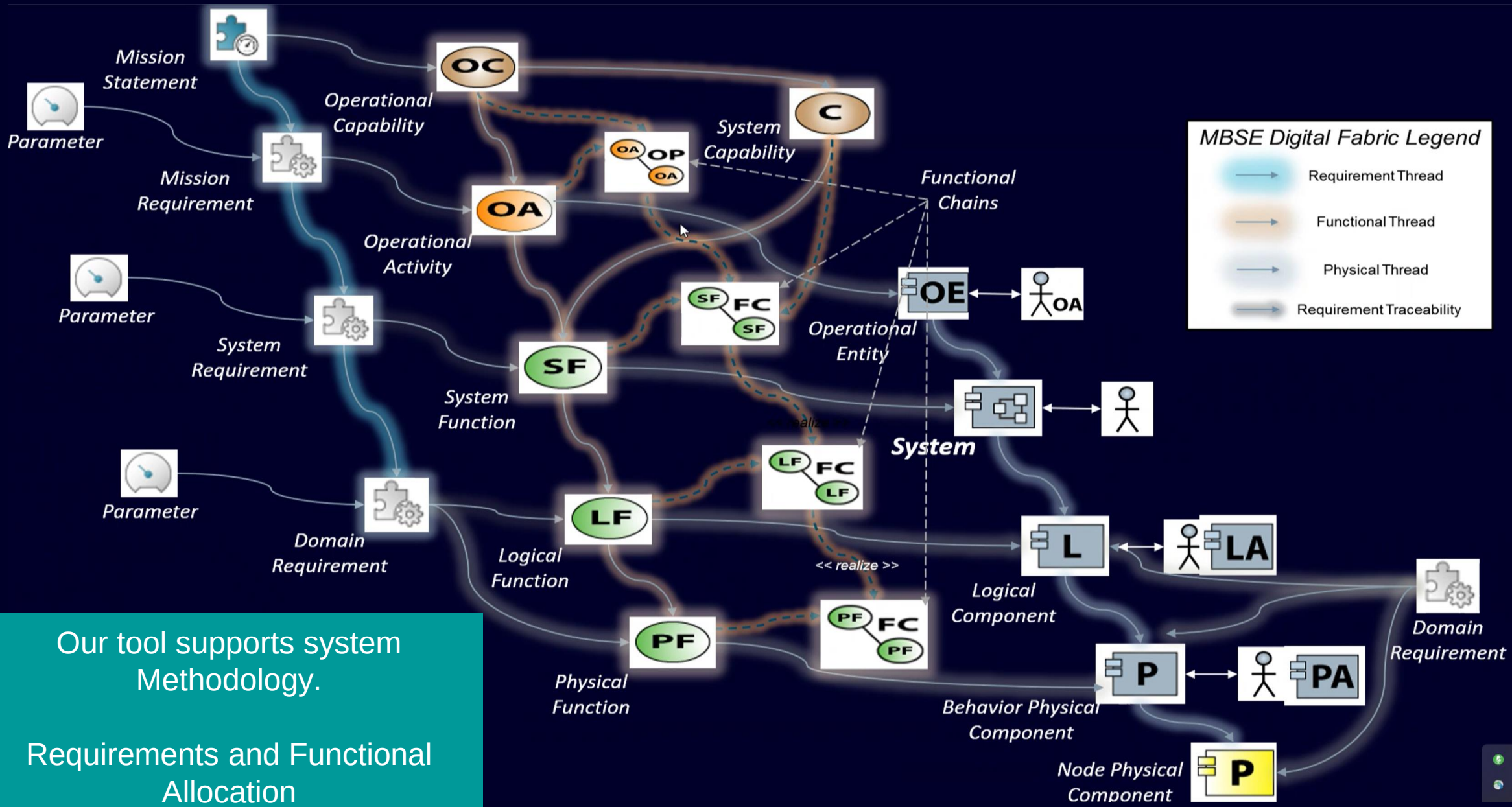

Our tool supports system Methodology.

Requirements and Functional Allocation

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Manage complexity
System to sub-system

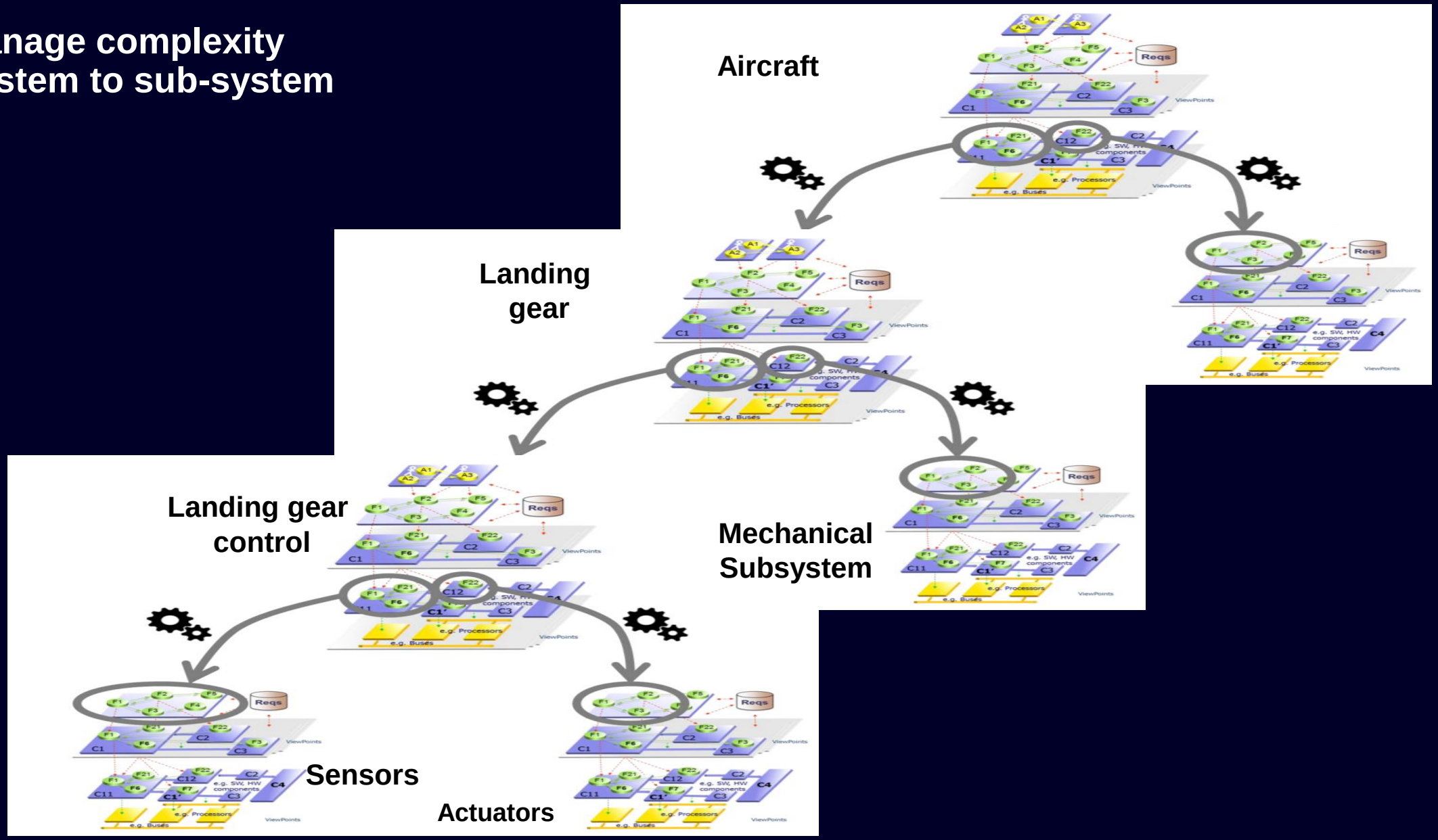
Aircraft is a system

Landing gear is a system

Landing gear control is a system

Landing gear control sensors is a system

Manage complexity
System to sub-system



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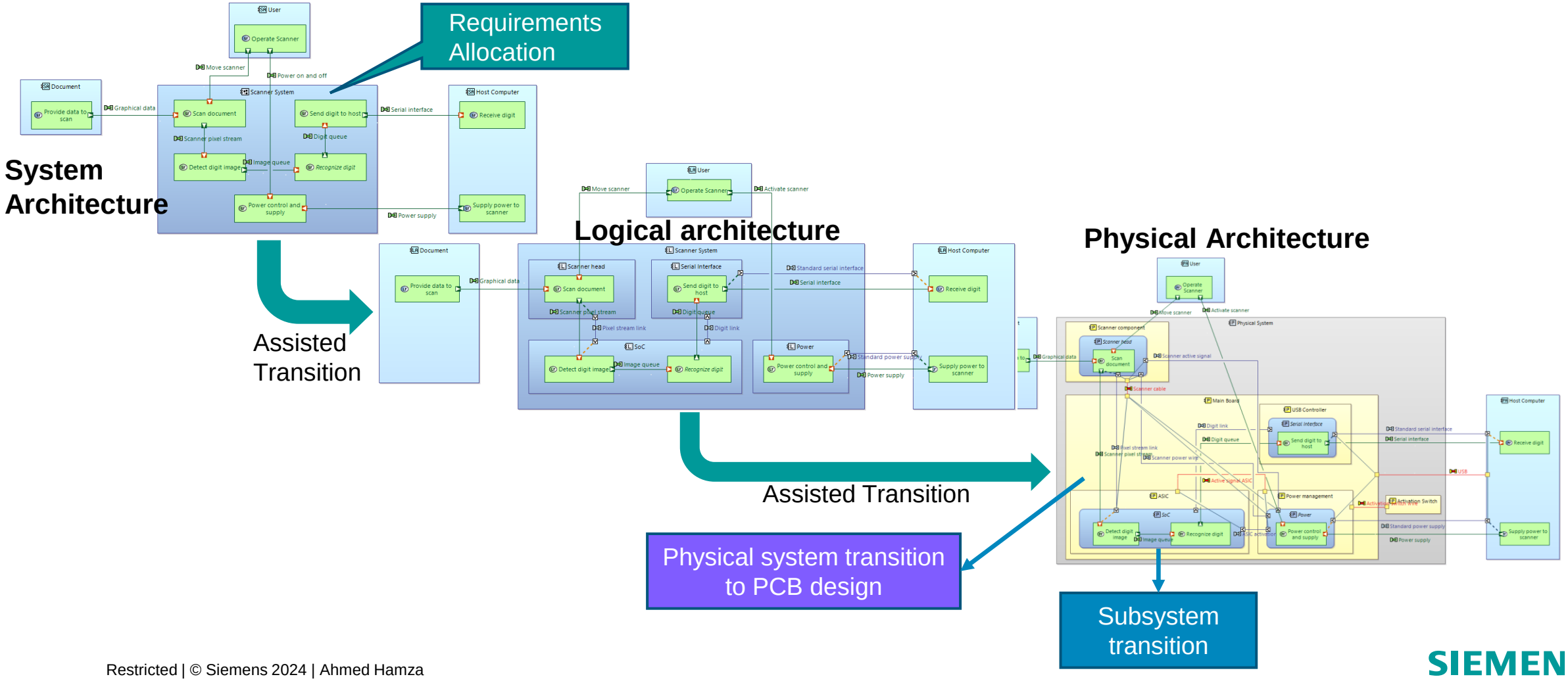
Compute Enclosure -level system exploration

Multi-Level system design using Arcadia methodology



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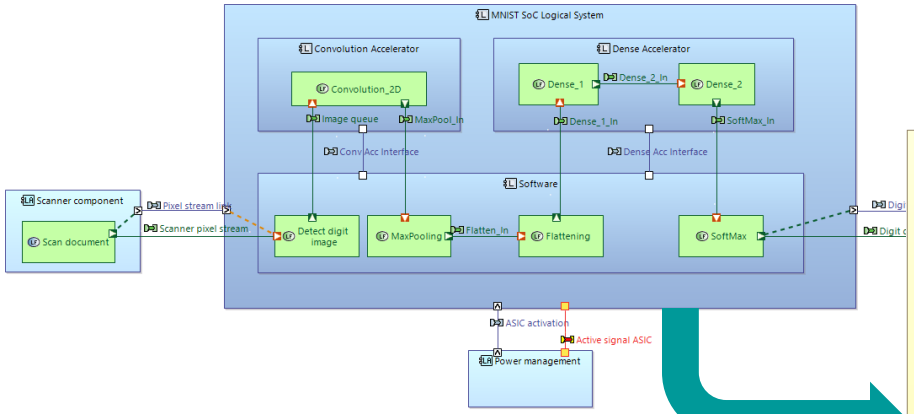
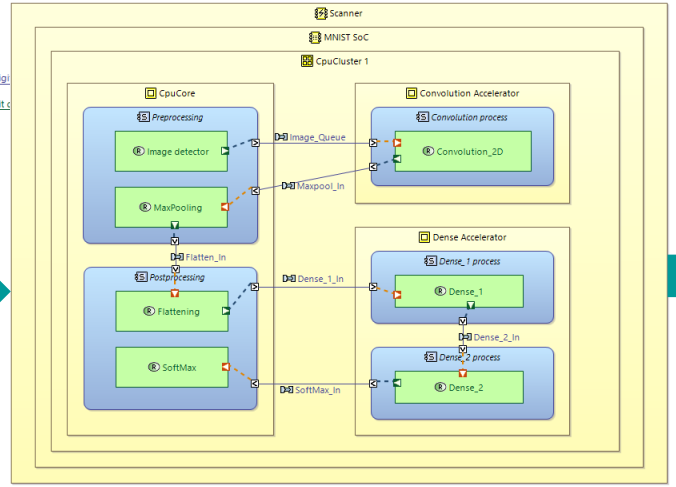
Performance analysis model

Creating a performance model based on the Physical or logical architecture

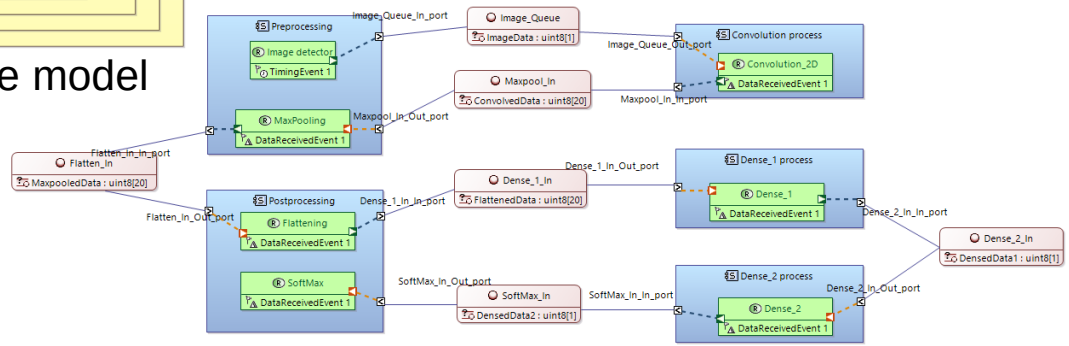


Manual design step



Subsystem performance model

Automatic model creation



Subsystem performance simulation model

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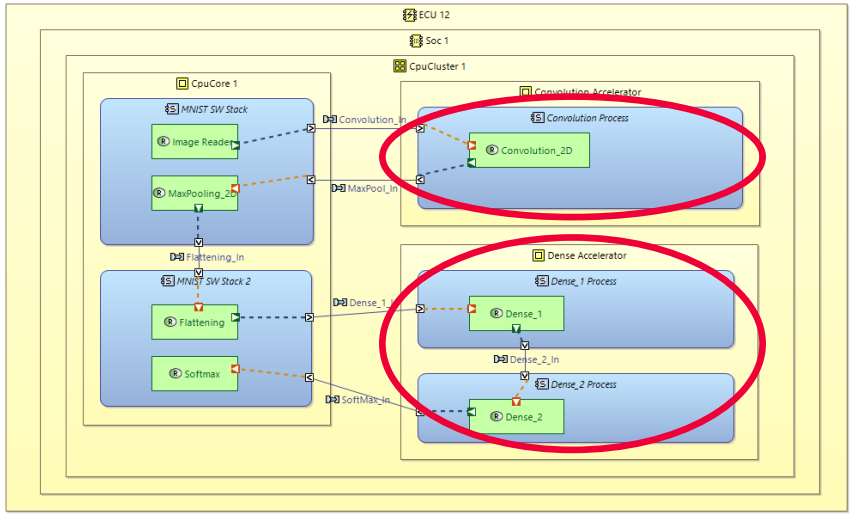
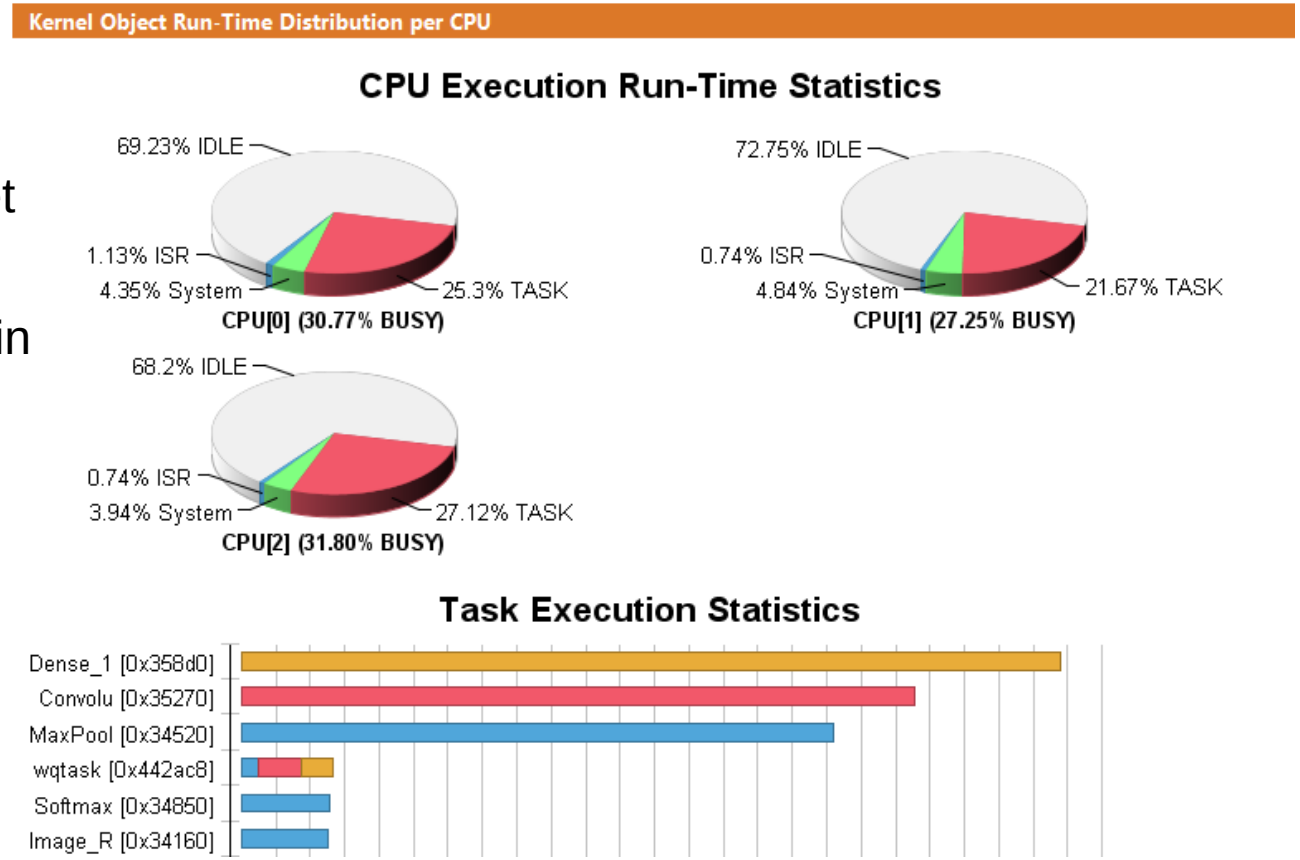
Analysis of parameterized performance simulation with two accelerators

Simulation with HW accelerator for convolution and Dense processes and 1 ARM Cortex A57 core

- Clock frequency: 500 MHz
- Data size between runnable tasks 1
- Interval between inferences: 20ms (target 20ms)

1. Convolution process reaches performance target
2. Dense processes reach performance target
3. CPU0 can handle all SW tasks with safety margin





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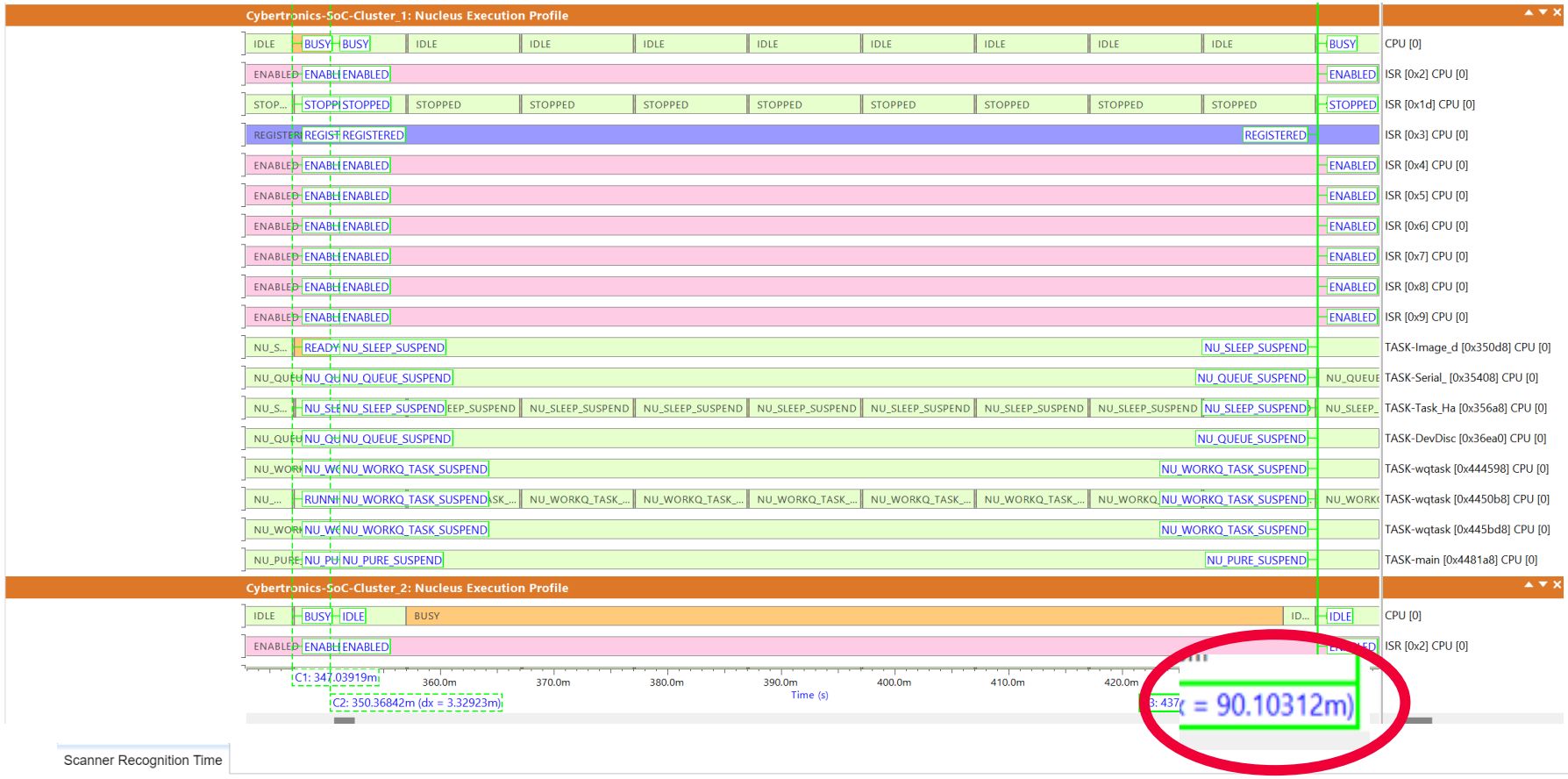
Architecture 1: Standard processor on PCB can’t meet the performance target



Next architecture will propose an ASIC is needed

Scanner Recognition Time

Model	Requirement	Parameter	Value	Min	Max	Certified By	Comment
Cybertronics Perf Model	2.0-2 The device shall recognize digits in a given time	Recognition time [ms]	90.13	15	20		Ran performance analysis based on using a standard CPU on the PCB. Measured value fails to meet budget by a large margin. Suggest creating a custom ASIC for this function.

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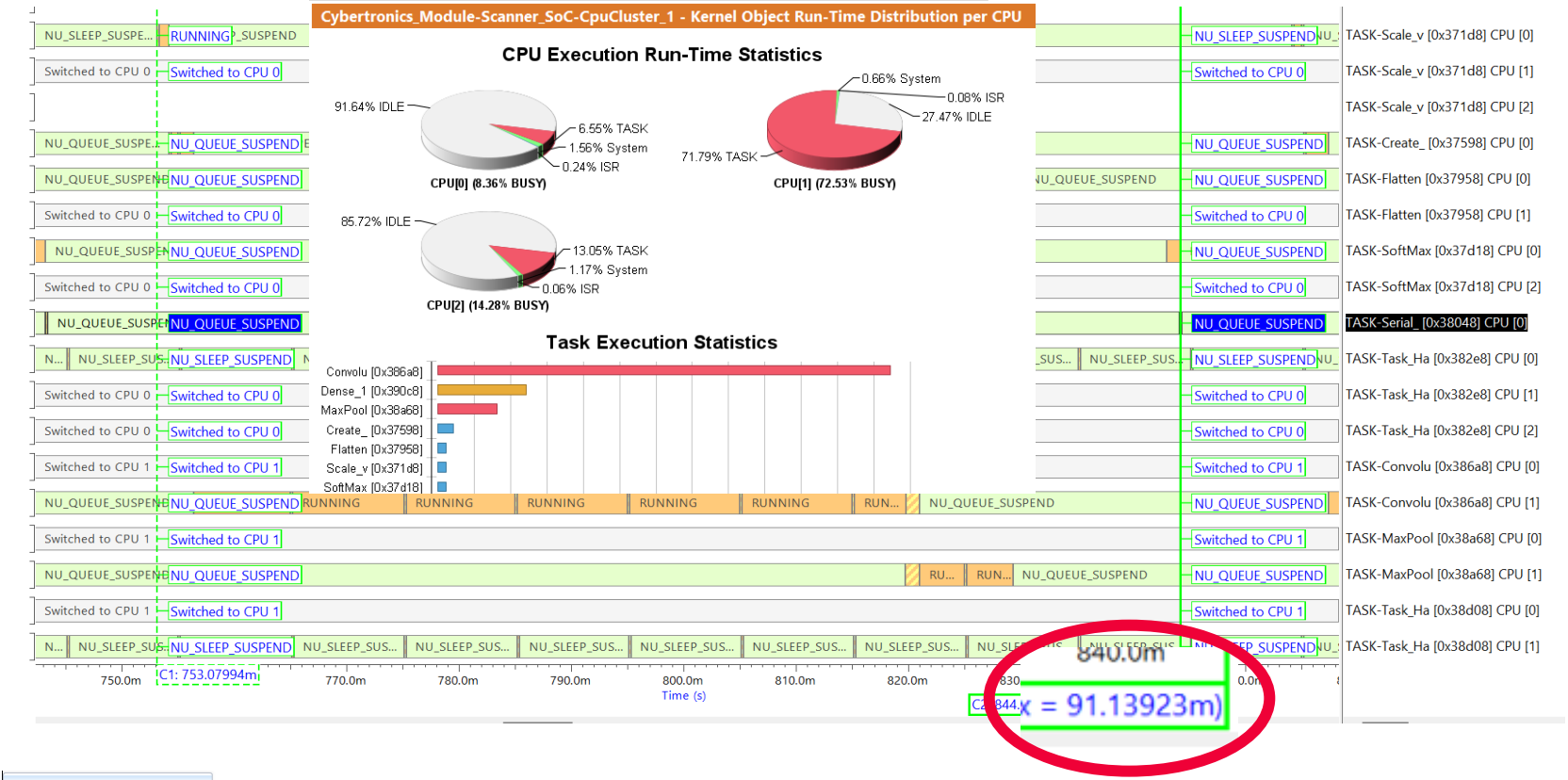
Architecture 2: SoC with 3 CPUs, and a full S/W implementation



Next architecture will propose a custom accelerator is also needed

Scanner Recognition Time

Model	Requirement	Parameter	Value	Min	Max	Certified By	Comment
Cybertronics Module	2.0-2 The device shall recognize digits in a given time	Recognition time [ms]	91.14	15	20		Simulated an SoC architecture with 3 CPUs, and a full s/w solution, but timing exceeds budget by ~5x. Analysis suggests accelerating convolution function.

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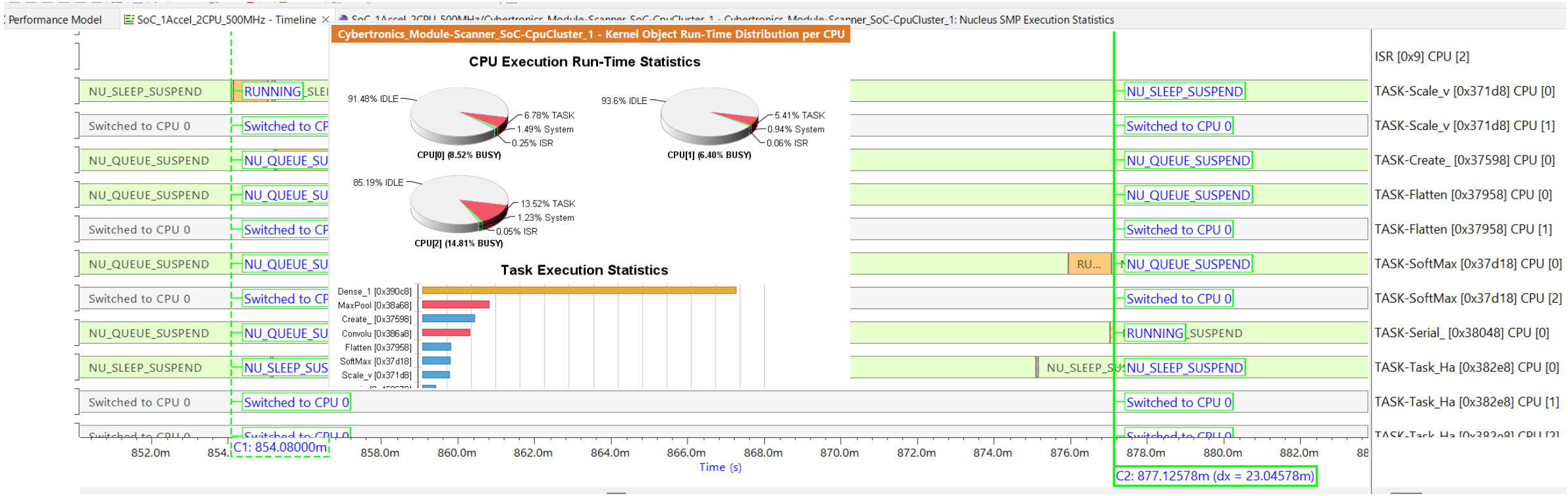
Architecture 3: SoC with 2 CPUs and 1 accelerator is still too slow



Scanner Recognition Time

Model	Requirement	Parameter	Value	Min	Max	Certified By	Comment
Cybertronics Module	2.0-2 The device shall recognize digits in a given time	Recognition time [ms]	23.05	15	20		Using an accelerator for convolution, but timing is still over budget by ~20%. Analysis suggests that we also need to accelerate the dense layer.

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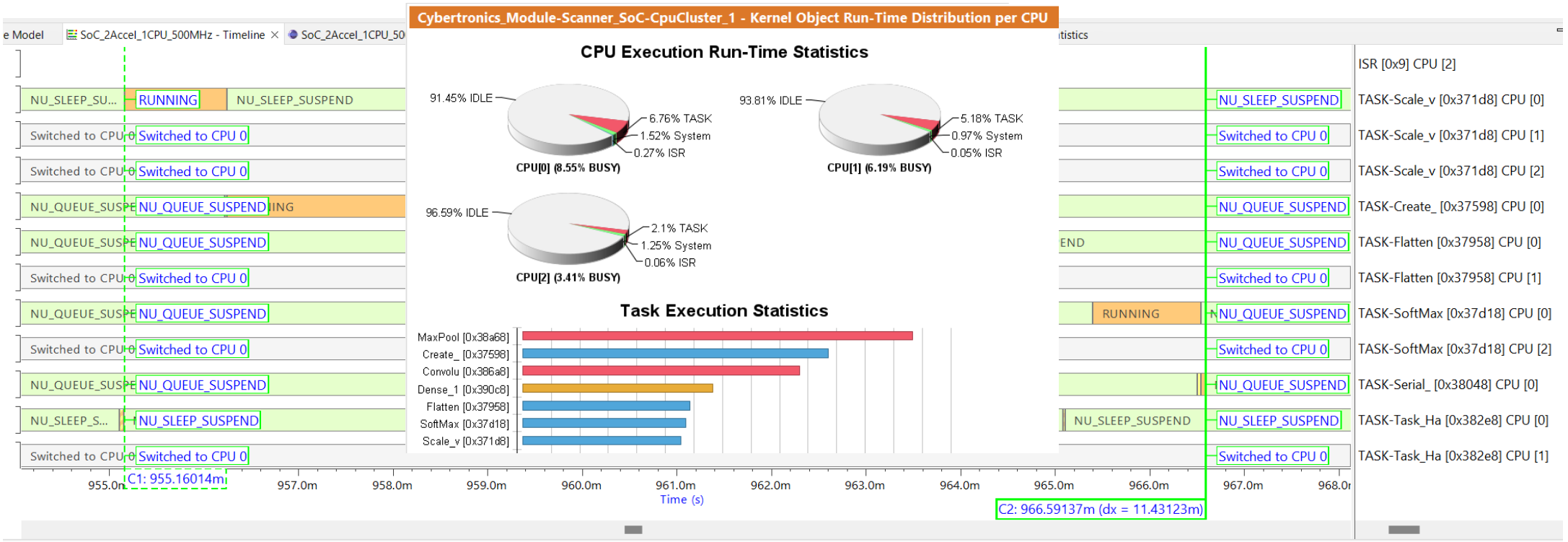
Architecture 4: SoC with 1 CPU with 2 accelerators can meet the timing requirement



Scanner Recognition Time

Model	Requirement	Parameter	Value	Min	Max	Certified By	Comment
Cybertronics Module	2.0-2 The device shall recognize digits in a given time	Recognition time [ms]	11.43	15	20		With acceleration of the dense layer also, the timing budget can be met. To be within min-max range we will constrain convolution accelerator to 5ms, and the dense layer to 2ms to achieve optimal timing.

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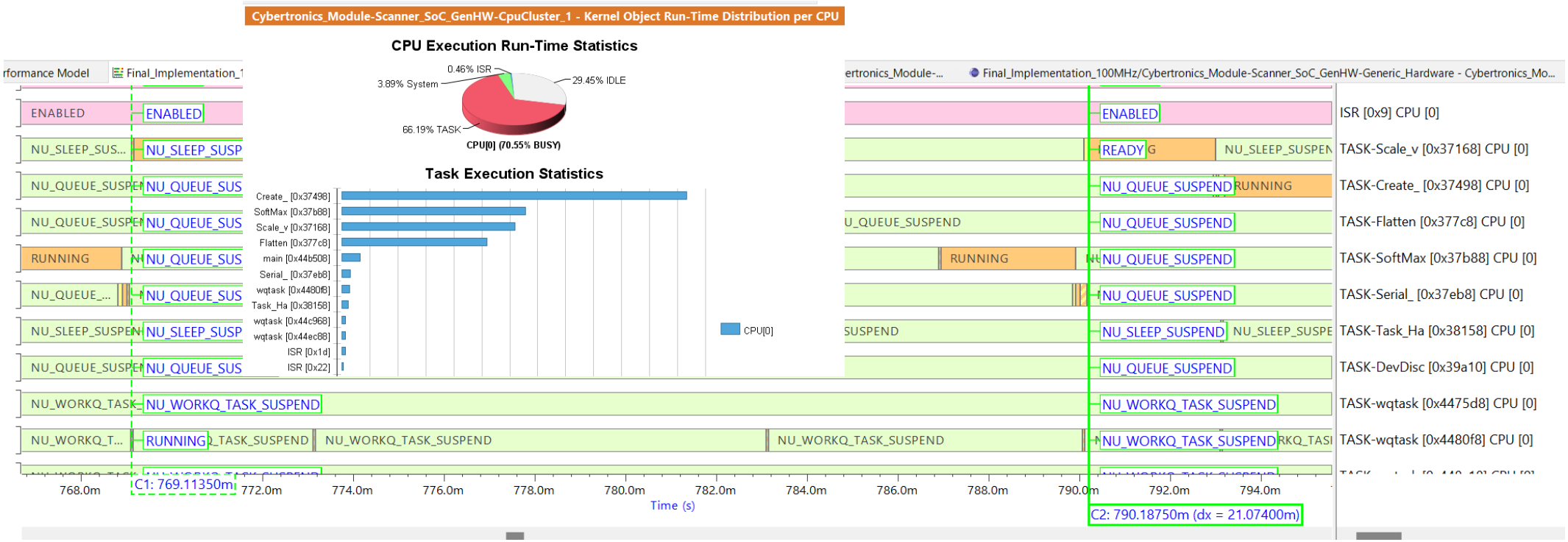
Experimenting with clock frequency: 100 MHz clock doesn’t quite meet the budget



Scanner Recognition Time

Model	Requirement	Parameter	Value	Min	Max	Certified By	Comment
Cybertronics Module	2.0-2 The device shall recognize digits in a given time	Recognition time [ms]	21.07	15	20		SoC with CPU plus 2 accelerators, simulated with 100 MHz clock frequency does not meet the requirement. Suggest we increase the frequency.

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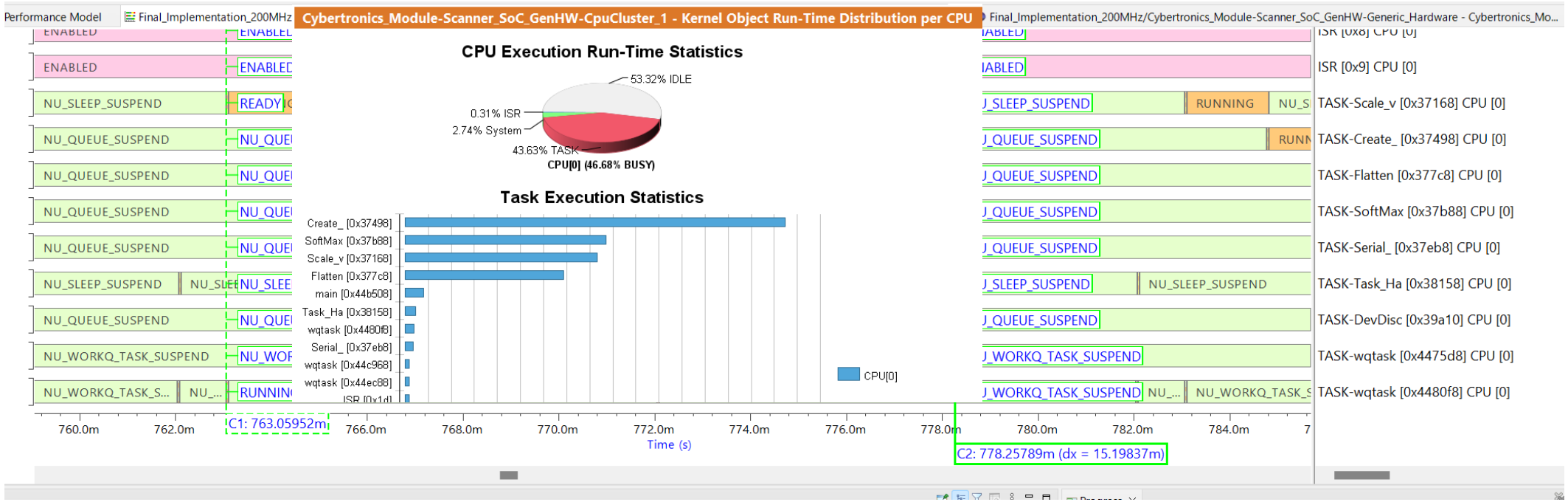
Experimenting with clock frequency: 200 MHz easily meets the requirement



Scanner Recognition Time

Model	Requirement	Parameter	Value	Min	Max	Certified By	Comment
Cybertronics Module	2.0-2 The device shall recognize digits in a given time	Recognition time [ms]	15.20	15	20	Lisa Verifier	SoC with CPU plus 2 accelerators, increased clock frequency to 200 MHz gets us within the budget, close to the minimum.

Performance simulation is successful, we're ready to move to virtual prototyping, and HLS flows!!

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MBCSE CORE Verification Threading: Summary

- The MBCSE CORE enabled us to establish a comprehensive digital thread, including:
  - Requirement allocation
  - Parameter usage in models
  - RFLP level transitions
  - Verification activity that captured the main project decision points / phase-gates

VCP	Parameter	Min	Max	Value	Comment	Version	Model	AE_Project	Config
Scanner Recognition Time	Recognition time [ms]	15	20	90.13	Ran performance analysis based on using a standard CPU on the PCB. Measured value fails to meet budget by a large margin. Suggest creating a custom ASIC for this function.	1.0.0	Cybertronics	Scanner Cybertronics Module_Perf	Cybertronics Module SW Only
Scanner Recognition Time	Recognition time [ms]	15	20	91.14	Simulated an SoC architecture with 3 CPUs, and a full s/w solution, but timing exceeds budget by ~5x. Analysis suggests accelerating convolution function.	1.1.0	Cybertronics Module	Scanner SoC	SoC_Full_SW_3CPU_500HMz
Scanner Recognition Time	Recognition time [ms]	15	20	23.05	Using an accelerator for convolution, but timing is still over budget by ~20%. Analysis suggests that we also need to accelerate the dense layer.	1.1.1	Cybertronics Module	Scanner SoC	SoC_1Accel_2CPU_500HMz
Scanner Recognition Time	Recognition time [ms]	15	20	11.43	With acceleration of the dense layer also, the timing budget can be met. To be within min-max range we will constrain convolution accelerator to 5ms, and the dense layer to 2ms to achieve optimal timing.	1.1.2	Cybertronics Module	Scanner SoC	SoC_2Accel_1CPU_500HMz
Scanner Recognition Time	Recognition time [ms]	15	20	21.07	SoC with CPU plus 2 accelerators, simulated with 100 MHz clock frequency does not meet the requirement. Suggest we increase the frequency.	1.2.0	Cybertronics Module	Scanner_SoC_GenHW	Scanner SoC GenHW 100MHz
Scanner Recognition Time	Recognition time [ms]	15	20	15.20	SoC with CPU plus 2 accelerators, increased clock frequency to 200 MHz gets us within the budget, close to the minimum.	1.2.1	Cybertronics Module	Scanner_SoC_GenHW	Scanner SoC GenHW 200MHz

Digital Thread and Verification Capture points

MBCSE Hardware and Software performance analysis

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Digital Thread

Tools flow ≠ Digital Thread
Tools flow ≠ Digital Twin

MBCSE solution:

- Normalize Threading across domains
- Normalize VCP* across domains
- Intelligent domain-to-domain threading
- Tools agnostic digital thread

The digital thread needs to be engineered.

A digital twin is an orphan unless connected to its digital thread.

* VCP: Verification Capture Points

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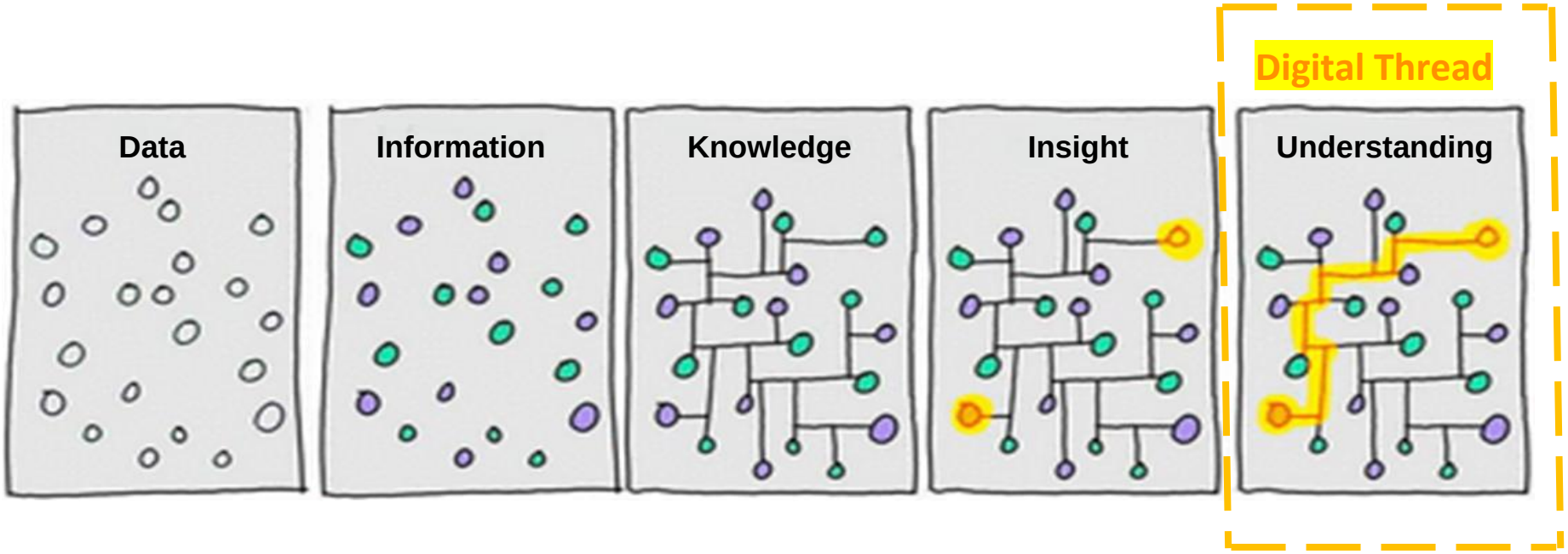
Digital Thread

What is the Digital Thread: It is a data communications framework that connects data flows. These data flows can be used to produce an integrated and holistic view of an asset's design data from physical and virtual systems



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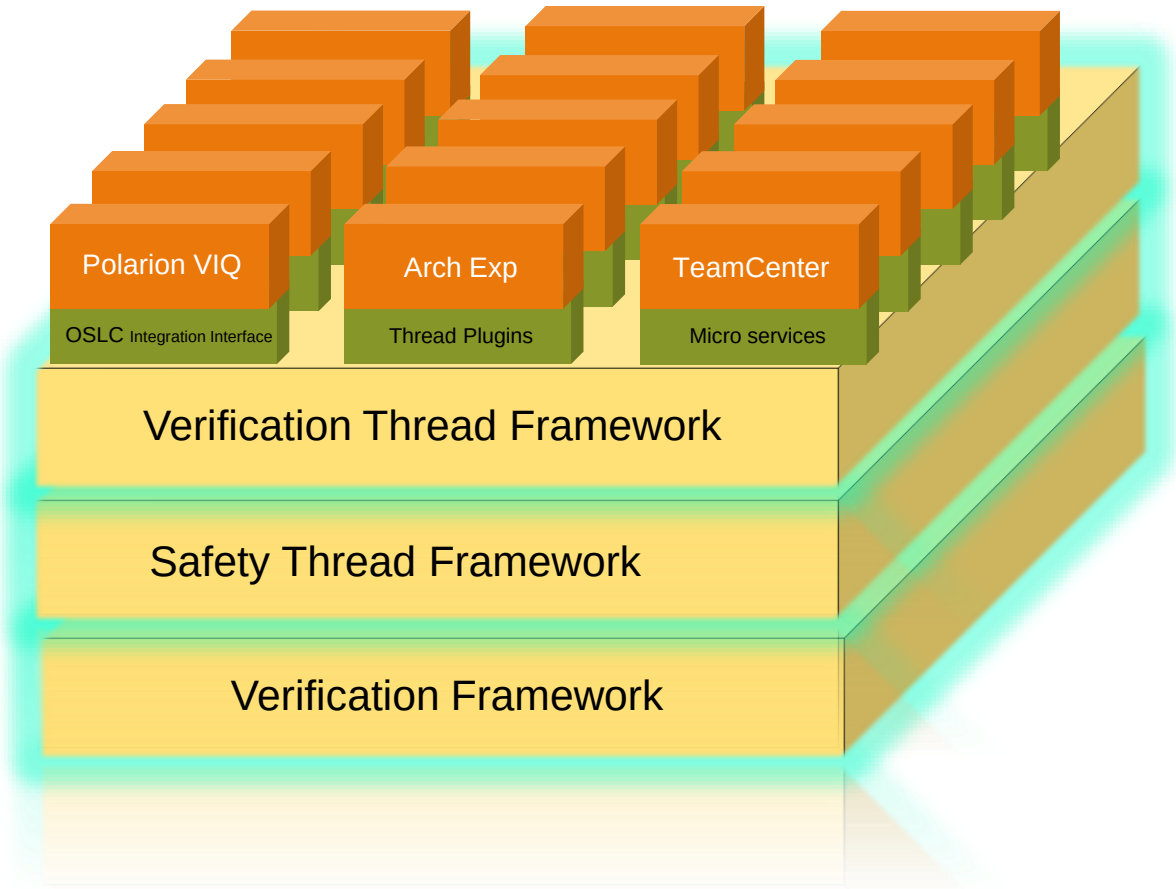
Threading Requirements & Verification Capture Points with the MBCSE CORE

- The MBCSE CORE allows key system artifacts, starting with parameterized requirements, to be added to a cybertronics digital verification thread
- Requirements from multiple sources such as DOORS, Polarion, Jira or even Excel spreadsheets can be mapped to the MBCSE thread model
- Link automation connects elements of threaded datasets based on defined rules that comprehend the methodology and conventions being used
- System models at any abstraction level can be added to the thread using tool plugins or integrations with code repositories such as gitlab
- As each requirement is verified, the artifacts that uniquely define the verification activity, such as test bench models, configuration files and saved results are captured on the thread
- Thread visualization and export of aggregated data from multi-order queries provide the ability to analyze the state of the project through the cybertronics development phase

Plug and Play digital thread

- Easley, add or remove tools from the digital thread
- Extend the ontology model for system design, system safety,
- Intrinsic system design verification and traceability framework



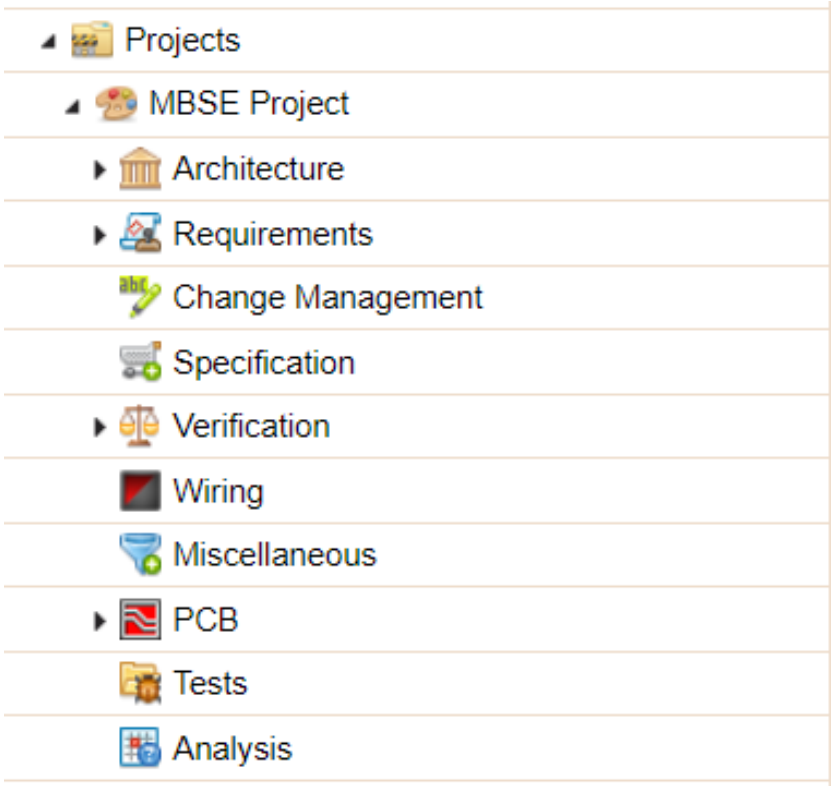
Eliminating Silos

DV Threader will link all project artifacts in one comprehensive view.

A project can link to different domains, technologies, and standards

Containers:

- Requirements
- Architecture
- Verification
- .
- .
- .
- Etc.



The list of containers is customizable based on technology and needs

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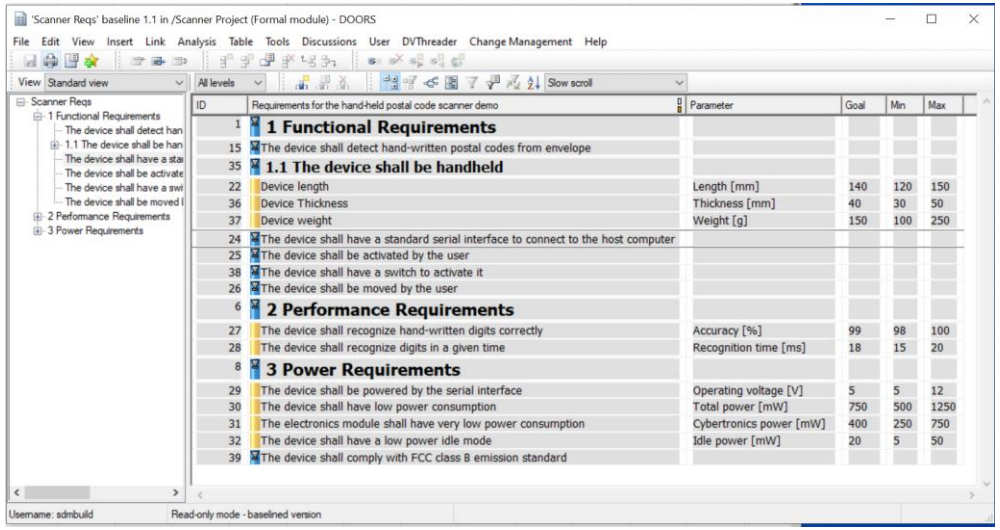
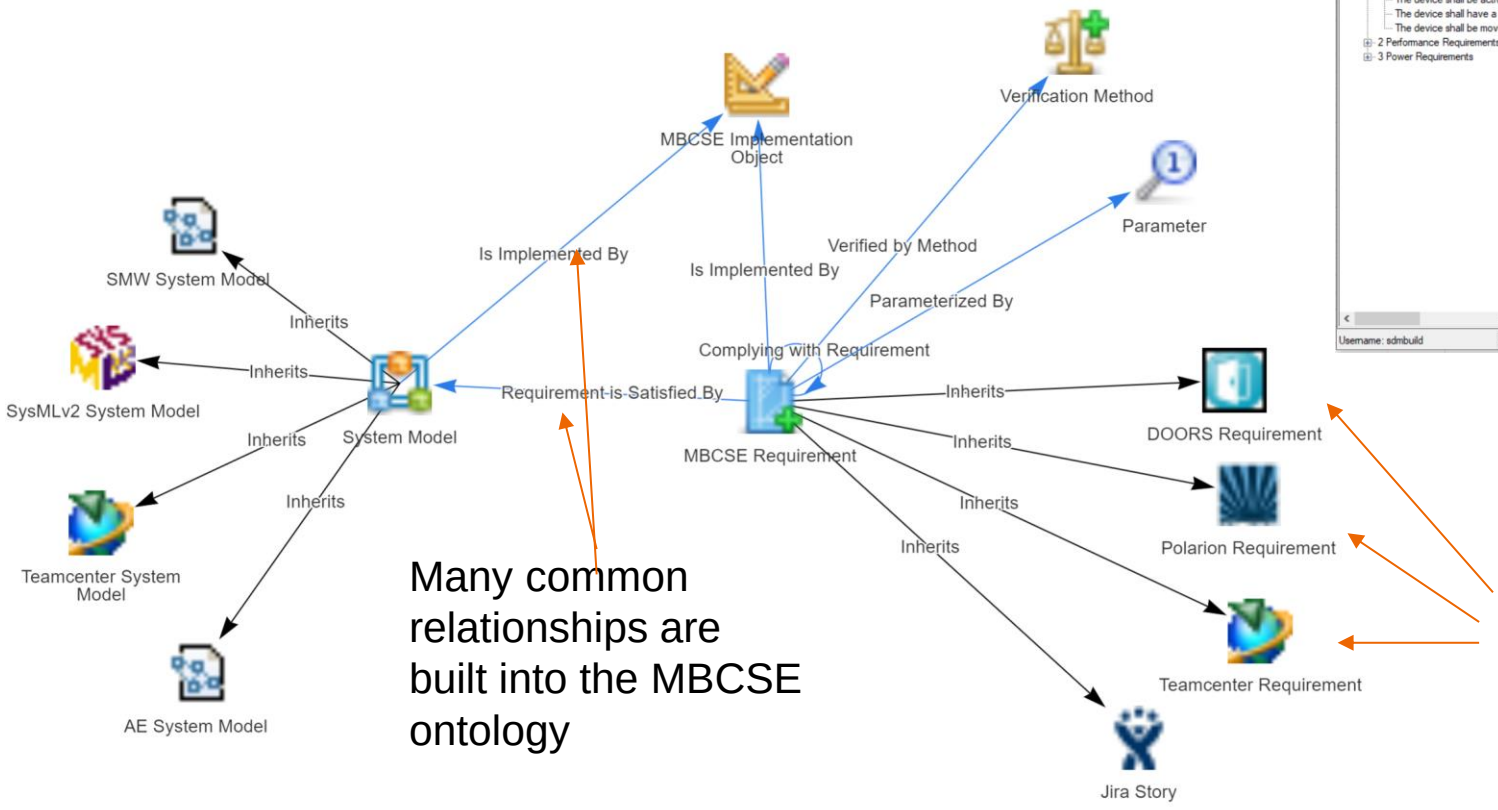
MBCSE CORE: Versatile Digital Thread – Repository Agnostic & Extendable

- Integrate data from multiple sources
- MBCSE threading model is independent of tool choices





Many common relationships are built into the MBCSE ontology

Any requirement tool can map onto a normalized requirement model

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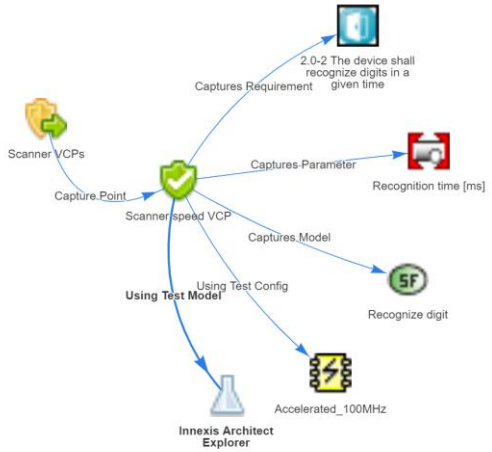
MBCSE CORE: Threading Verification Capture Points

- Capture requirement verification activity through all stages of the design process
  - including the failures that lead to changes in approach
- Record each instance where the requirement was deemed to be verified
  - and the precise model versions and test configurations



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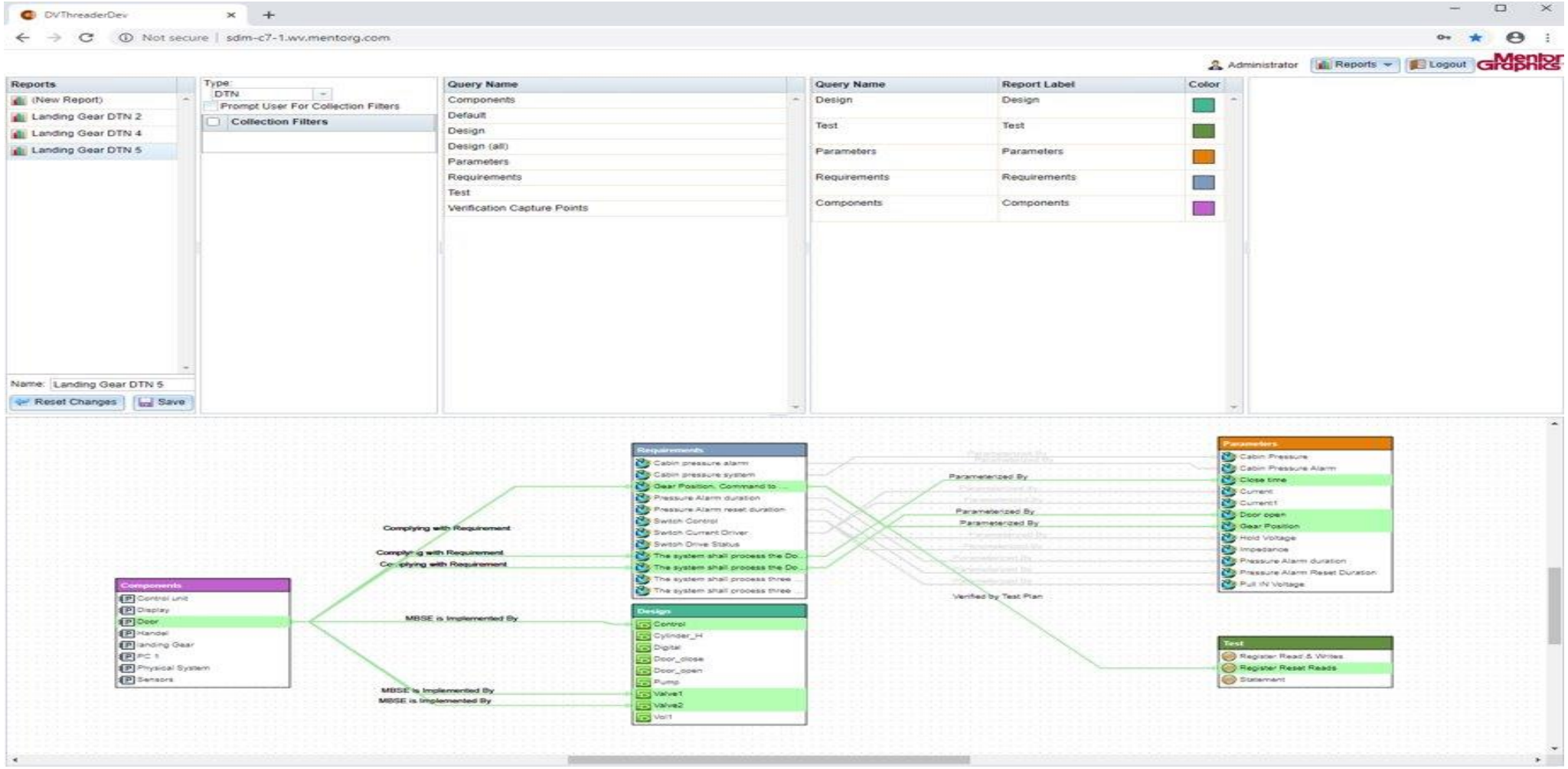
View a digital Thread



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Demo

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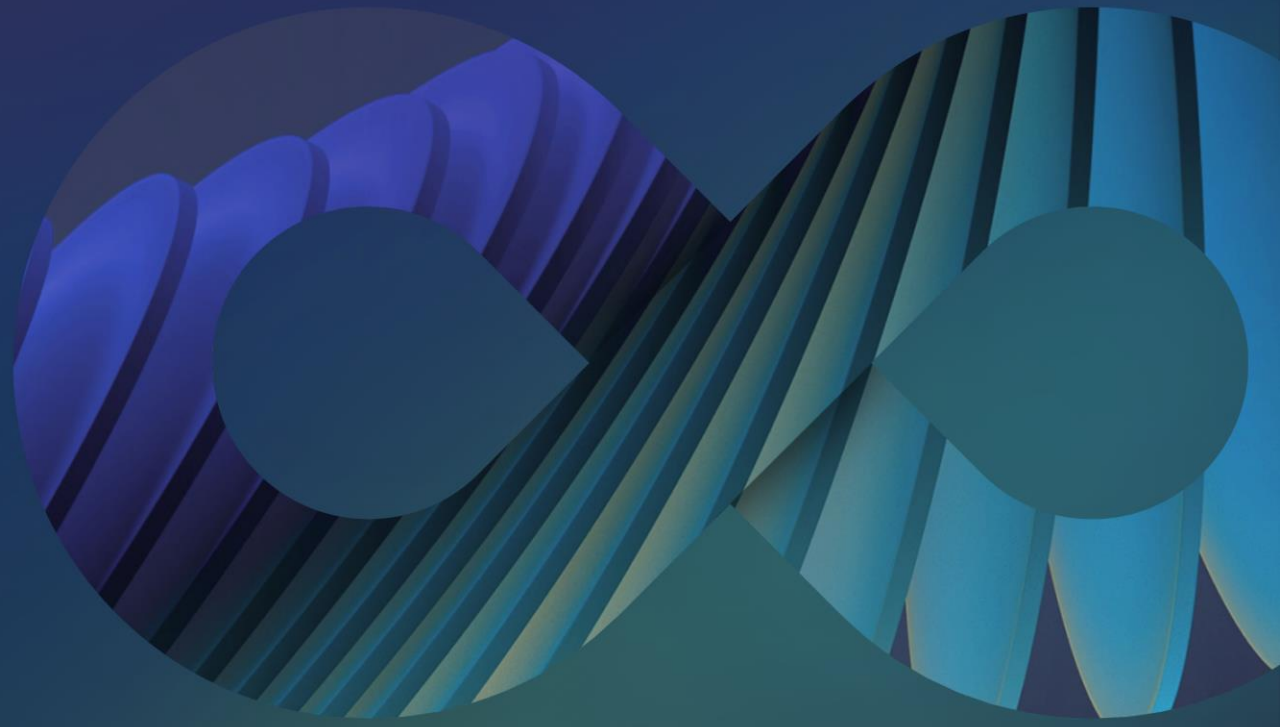
Contact

Ahmed Hamza



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