Validation with Simulation

Hatley-Pirbhai Control Flow Diagram with SysML for Early Validation

Hatley-Pirbhai

- Hatley-Pirbhai (H/P) is one of the most functional analysis methods used in systems engineering [1, 2, 3].
  - Despite perceived as an outdated modeling approach [4].

- The most useful and common models in H/P are Context Flow Diagram (CFD), Data Flow Diagram (DFD), and Control Specifications (CSPEC).

- Graphical representations are not enough to support complex systems.

- H/P is outdated, but not obsolete.

Hatley-Pirbhai Control Flow Diagram with SysML for Early Validation

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Abstract. Although CFD/DFD is one of the most used diagrams in the Hatley-Pirbhai (H/P) modeling method, H/P does not offer the semantics to support the execution capability of behavioral modeling. In the cyber-physical systems that operate in an open environment, an executable model is necessary to perform simulation for early phase validation. This study proposes a method for providing the execution capability by improving H/P using SysML with the MBSE Object-Oriented context. SysML is supported by the fUML execution engine that has been standardized by the Object Management Group (OMG). With this standardized platform, the simulation results are more precise, consistent, and less ambiguous, which are necessary to perform better validation. The results showed that SysML diagrams maintained model readability and could easily implement the H/P method com-

Hatley-Pirbhai Limitations for Simulation

1. Offers no semantics for defining dynamic data relationships [1].

2. No formally defined semantics to support simulation for an early dynamic analysis in the development phase [3].

3. DFD does not define the execution order [5] and concept of time [6]. As a result: No loop [7] or Conditional node [8, 2].

4. Does not visually distinguish between time-continuous & time-discrete signal [3].

Requirements Validation in Early Phase

Discipline Engineer

System Engineer

Save time and cost

Validate the logical consistency of the model
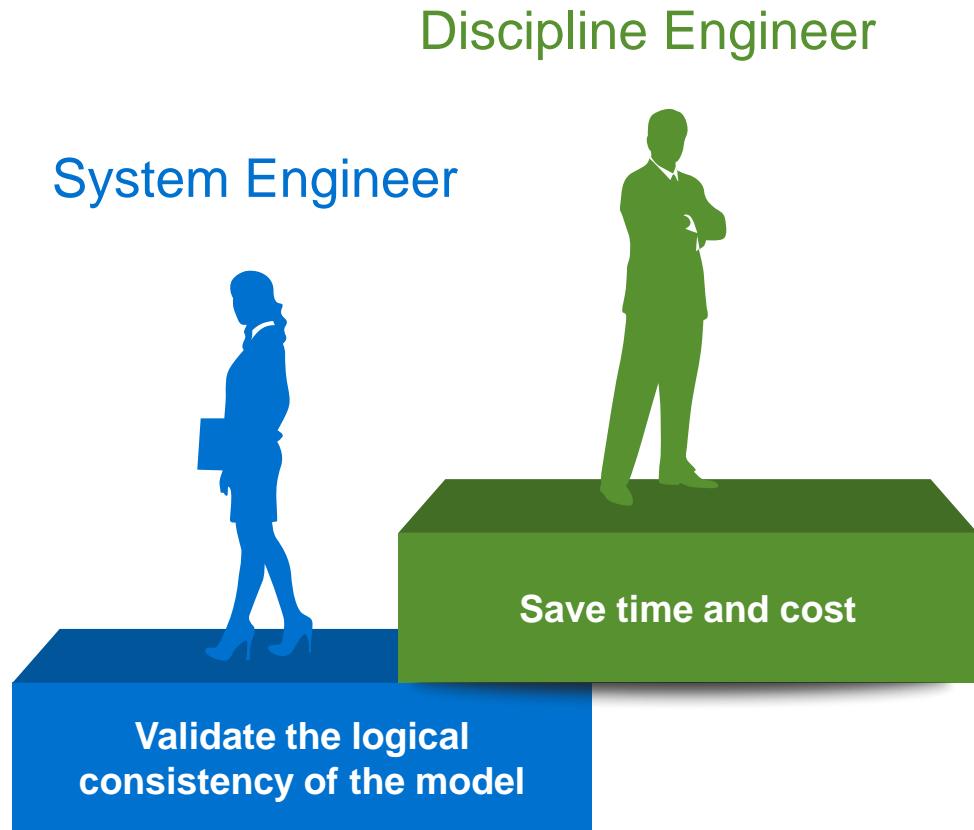
- Validate the logical system behavior model for consistency and rationality on requirements in the early phase.
  - Simulation of the behavior model captured in the analysis phase can accurately helps describe the complex working conditions of the features and validate the rationality of the requirements model [9, 10].

- Early phase requirements validation can save time and cost.
  - Performing full validation of the state migration logic correctness in the early phase can save time & cost [9, 10, 11].

Objectives of the Study

- To improve the H/P methodology, which has been widely adopted by the industry, by replacing the H/P CFD/DFD with SysML to complement the behavioral modeling and execution capability.

- To leverage the engineer knowledge on H/P toward MBSE adoption.

Methodology

act [Activity] Methodology [Methodology]

- Mapping H/P Elements to SysML Elements
- Building UML Profile and Stereotypes for Hatley-Pirbhai
- Modeling H/P Diagrams with SysML Diagrams using the Profile
- Performing Simulation with fUML Engine
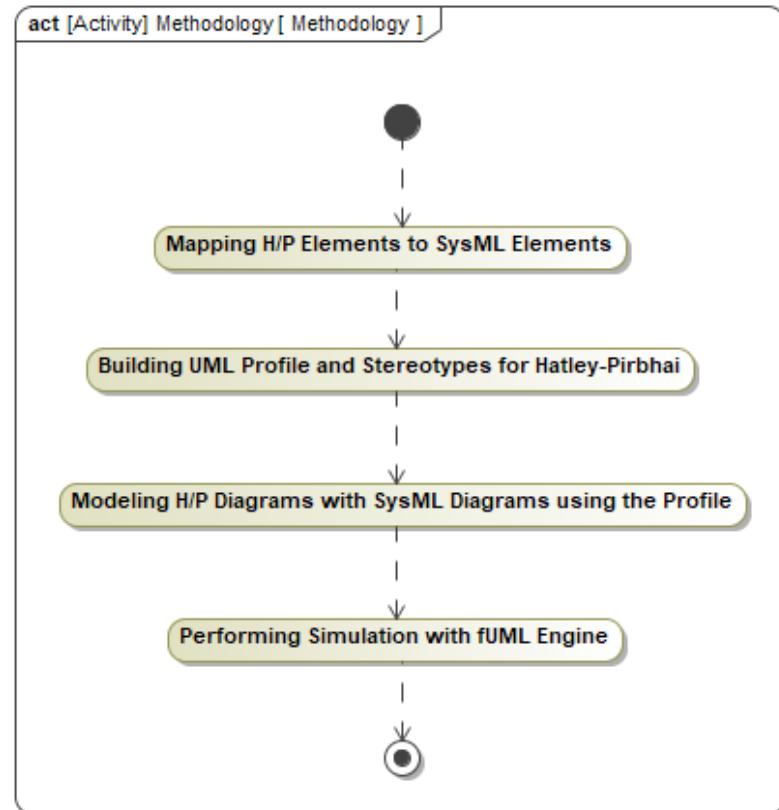
Step 1 — Mapping the H/P CFD/DFD concept with SysML

Step 2 — Model the H/P Concept as UML Profile
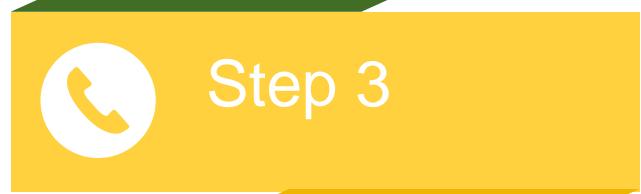
Step 3 — Perform H/P for Control Flow & Data flow analysis with SysML Activity diagram
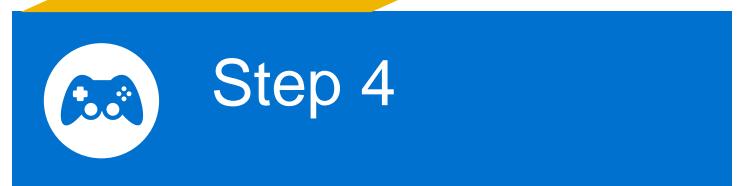
Step 4 — Validate Requirements with Simulation

Step 1: H/P Elements to SysML Mapping

| H/P Elements	SysML
Feature Context	Block
Feature	Block
Terminator	Block
DataStore	Block
Process	Activity
CSPEC	State
Signal	Signal
State to Process • Activate Process • Disable Process	State to Process • Dependency • Dependency
Control Flow	Connector, Control flow
Data Flow	Connector, Object flow

Step 2: Model H/P UML Profile

- Model the H/P concept to SysML mapping as a UML profile.
- This H/P Profile will be used to extend the Standard SysML model element with the H/P concept which allows the System Engineer to model the system behaviour based on the H/P concept and methodology.
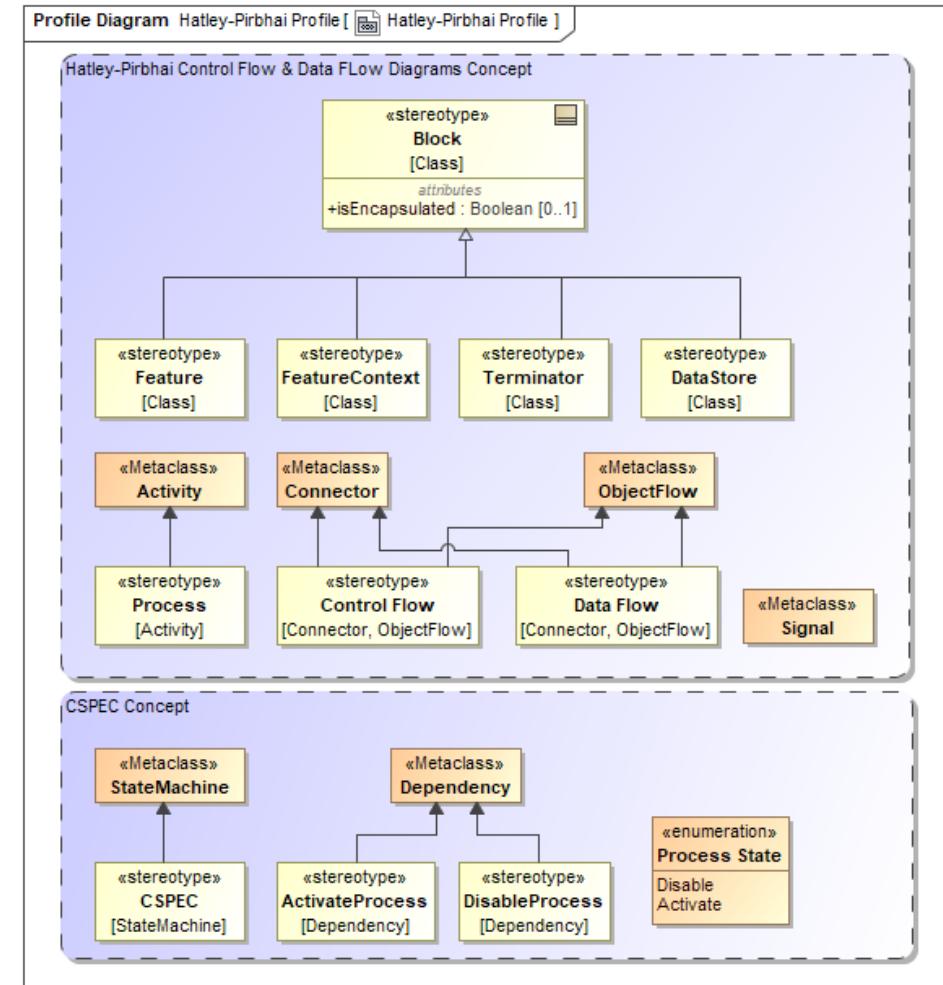
Step 3: Model H/P Behavior with SysML

- Based on the H/P Profile, extend the SysML with both CFD/DFD concepts in the Activity diagram.
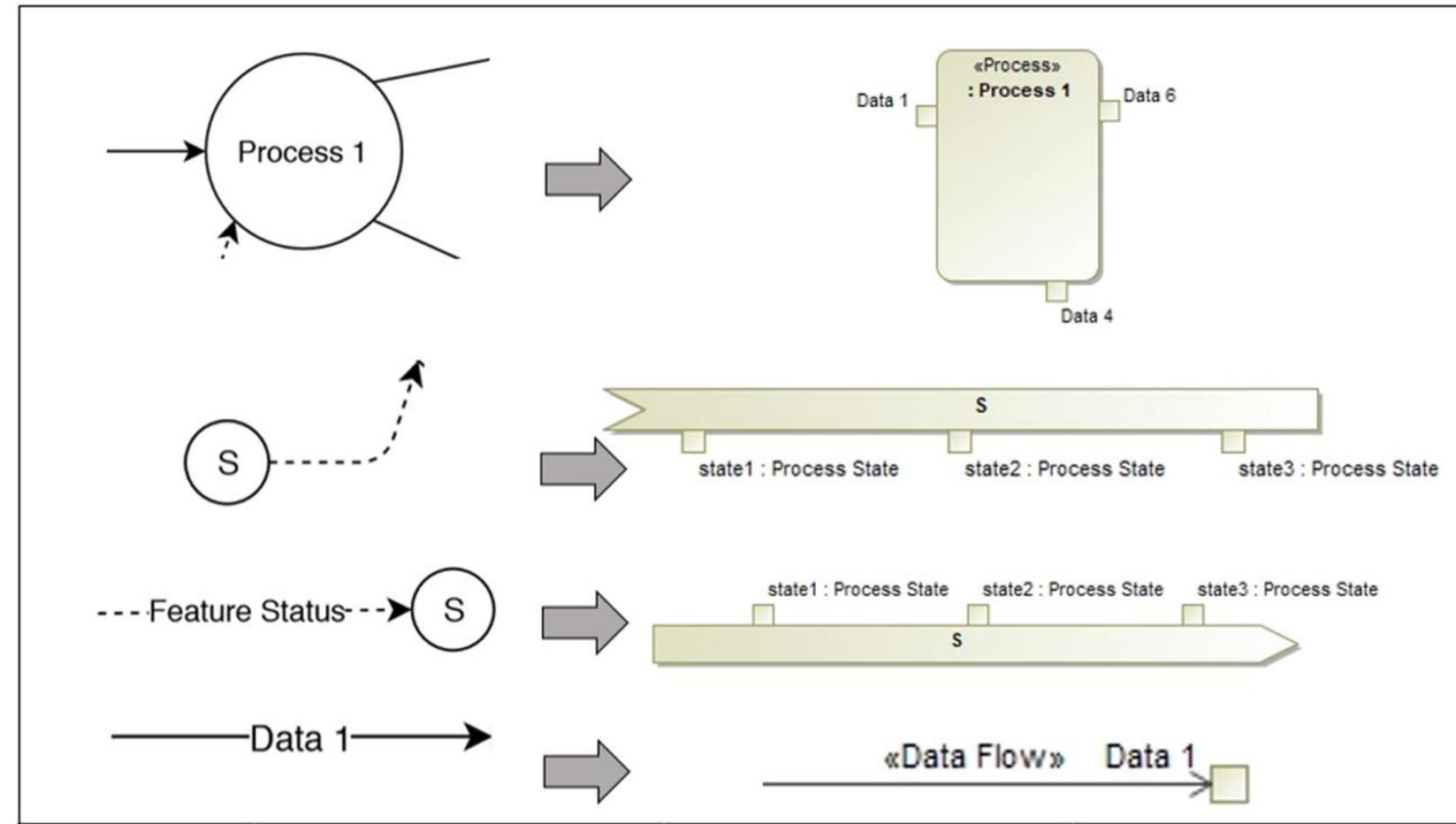
# Step 3: Model H/P Behavior with SysML

- H/P State element will be modeled as a SysML State Machine.
  - H/P State Transition will be modeled as a SysML State Transition.
  - SysML State transition supports Signal Event, Call Event, Change Event, and Time Event trigger.
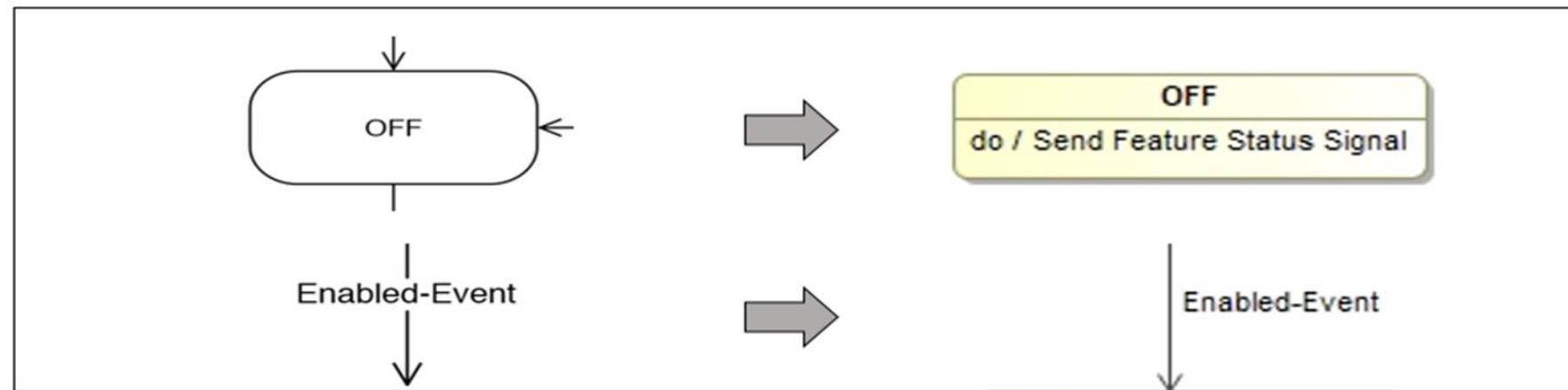
Step 4: Model the System and Simulate

- Start our system analysis with H/P Concept in SysML.
- Upon modeling the system behavior based on the Moore automata control logic in CSPEC STD,
  - Perform simulation for requirements validation by executing the model that has been built.
- The system model simulation can be run by using any simulation engine that supports the fUML specifications.
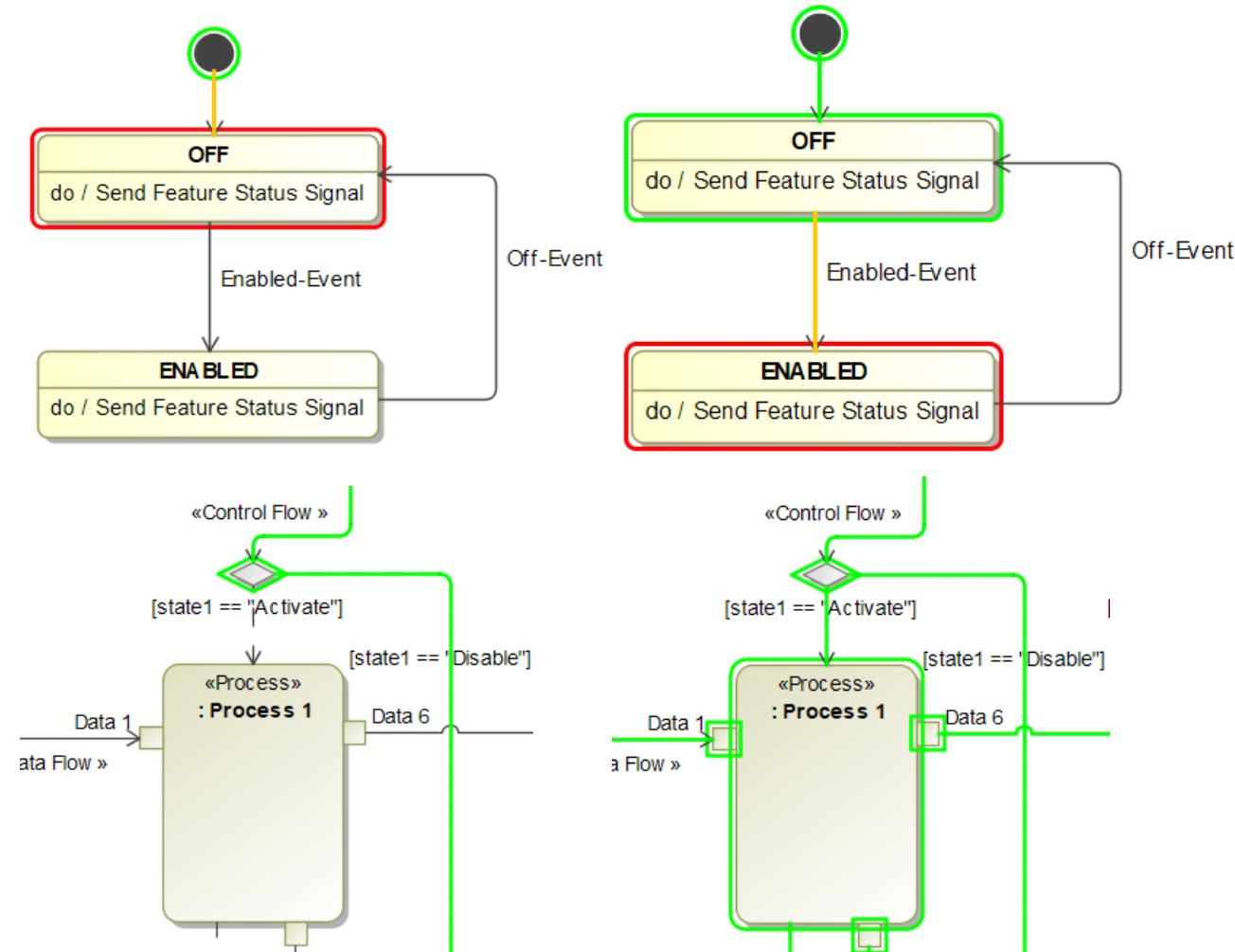
# Implementation of CSPEC STD with SysML State Machine Diagram
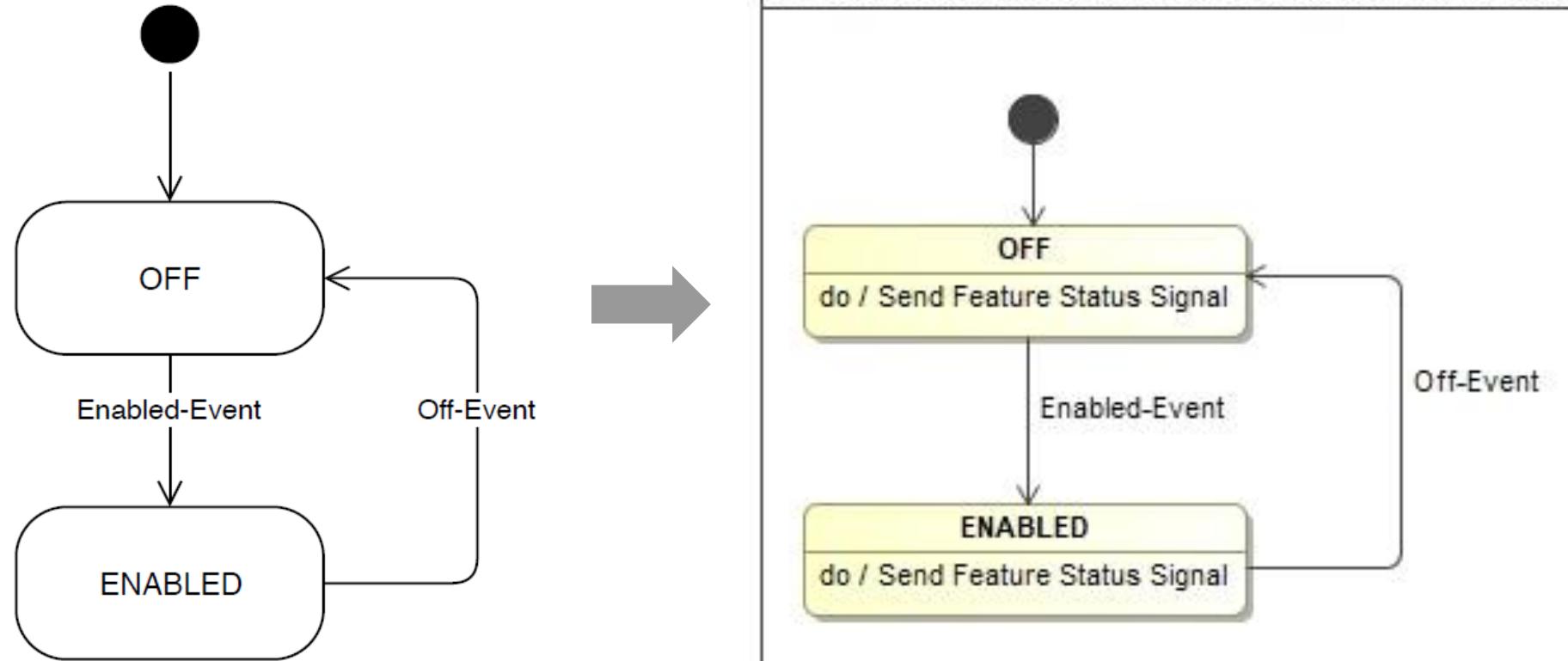
Implementation of CSPEC PAT from States to Processes Dependency Matrix

Input	Process		
Feature Status	**Process 1**	**Process 2**	**Process 3**
OFF	Disable	Disable	Disable
ENABLED	Activate	Activate	Activate

| #	▽ Feature Status	Process 1	Process 2	Process 3
1	OFF	Disable	Disable	Disable
2	ENABLED	Activate	Activate	Activate
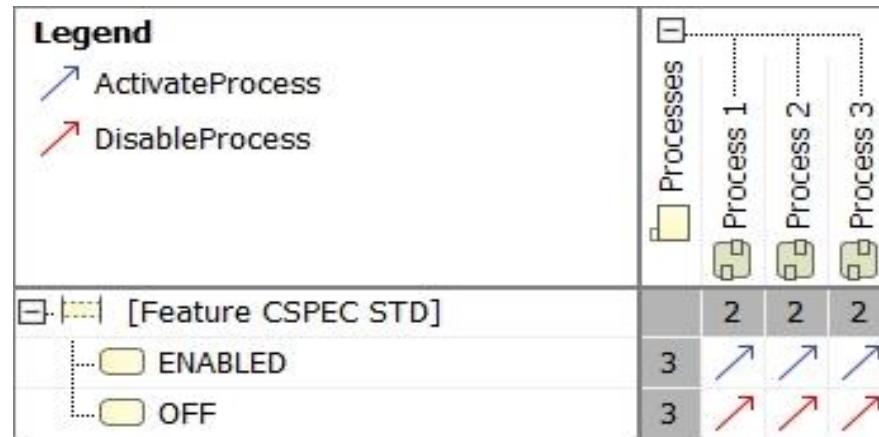
CSPEC STD States to CFD/DFD Processes Dependency Matrix

Implementation of CFD/DFD with SysML Activity Diagram
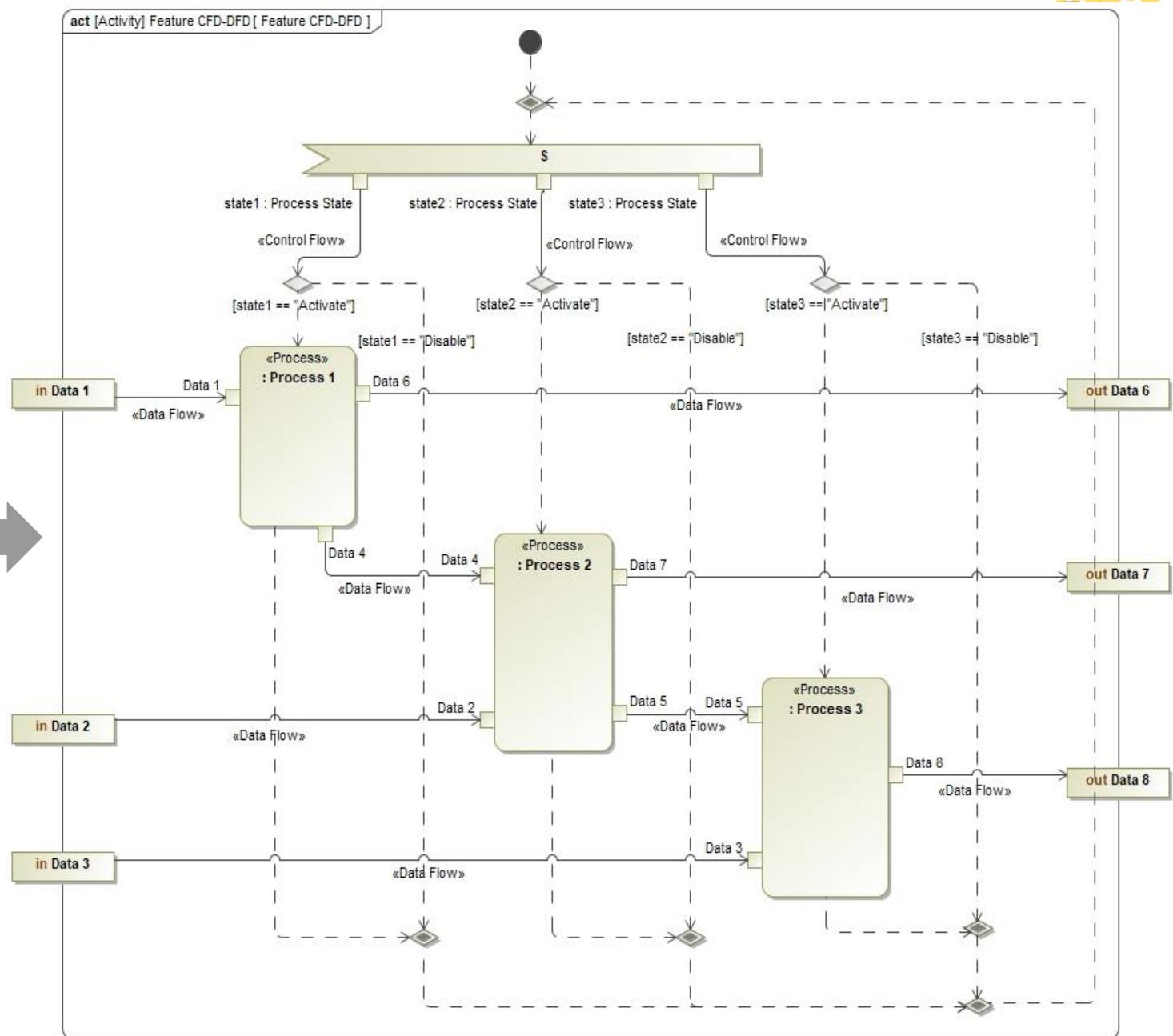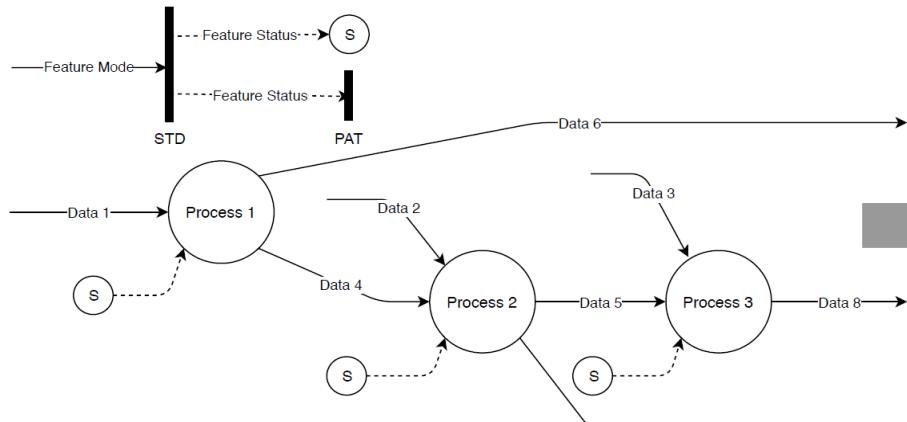
Simulation of CSPEC STD and DFD
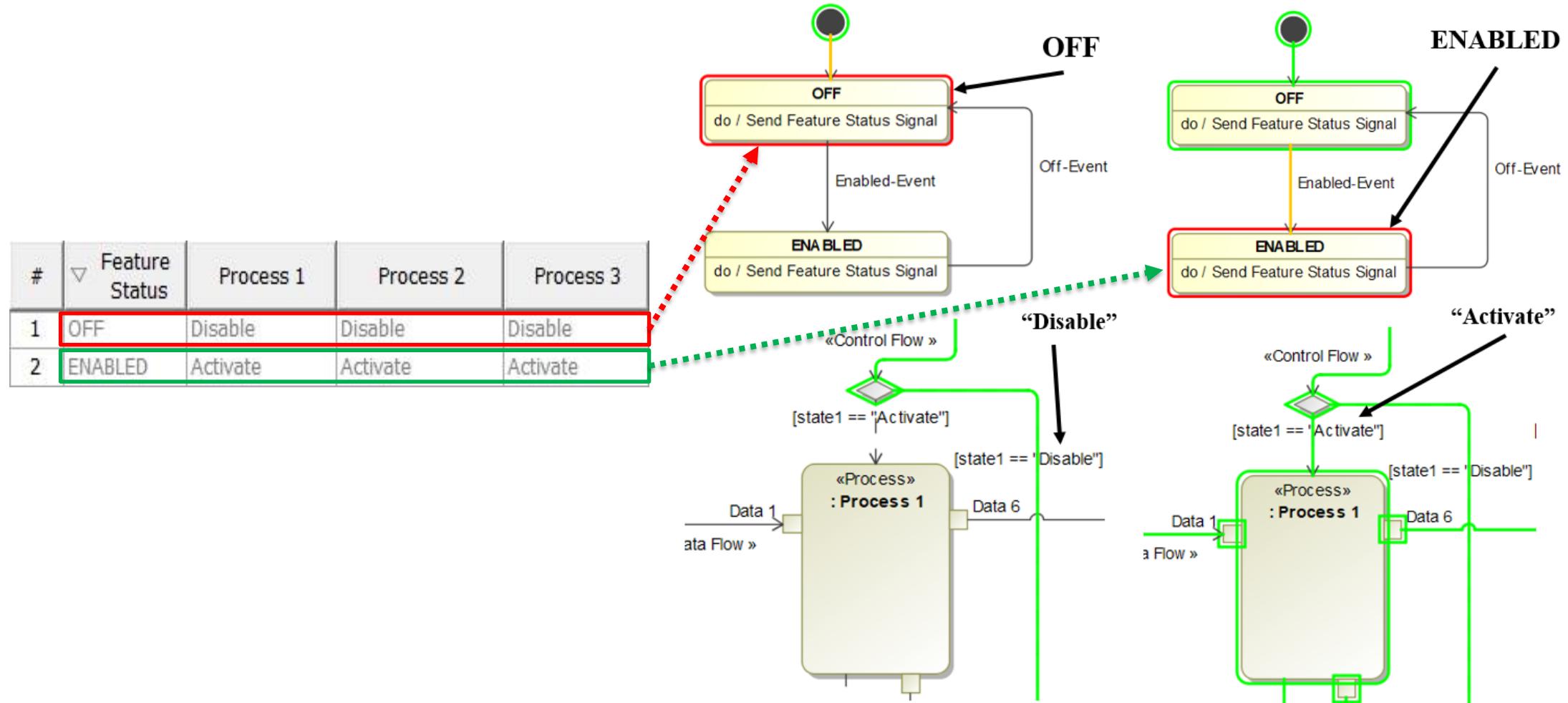
Conclusion

- The execution capability of the SysML Activity diagram, functional analysis on the feature control logic can be performed in the early phase and can be validated easily by the stakeholders even though it is still on the high-level of abstraction [13].

- The capability to run simulations in the early phases of development is helpful in the cyber-physical systems that operate in an open environment such as self-driving cars and other systems in the automotive domains.

Future Work

SysML Sequence Diagram for a comprehensive functional analysis since it is a more precise specification of behavior that is well-suited to serve as a detailed design artifact [13].
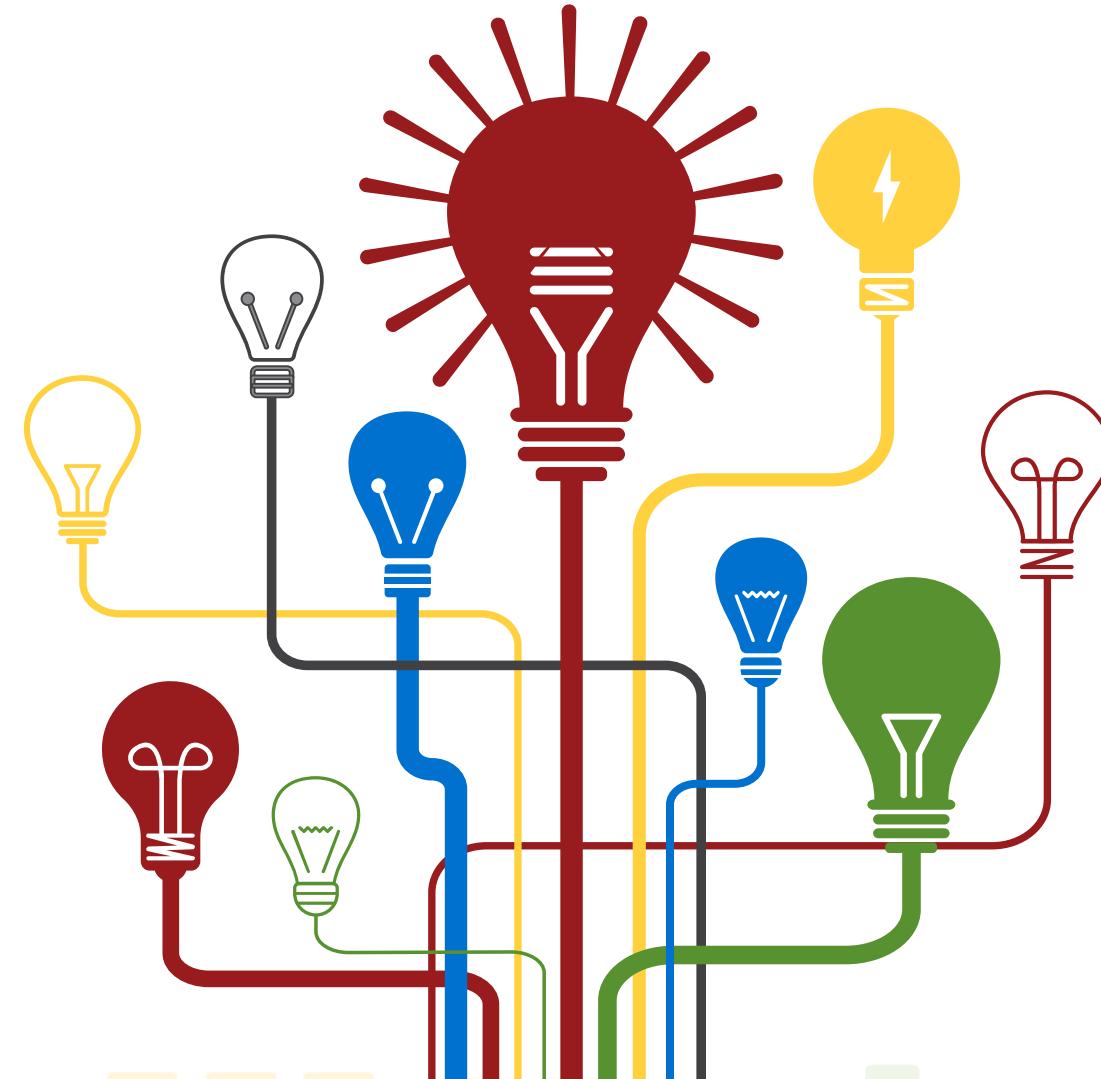
Automata design of Hatley-Pirbhai Control Specification State Transition Diagram (CSPEC STD).
In Mealy Automata, both the present state and input can affect the result of the next state of the state machine [2].

Reference

- [1] Maier & Rechtin 2009
- [2] Baresi & Pezzè 1998
- [3] Wood & Wood 1989
- [4] Pressman 2010
- [5] Fuggetta 1993
- [6] Yang 2005
- [7] DeMarco 1978
- [8] Hathaway 2019
- [9] Gibson 2001
- [10] Fuggetta 1993
- [11] Maurer & Winner 2013
- [12] Karban, Jankevičius & Elaasar 2016
- [13] Delligatti 2014

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